Nanoelectronics Overview

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Nanoelectronics

Definition: Digital and signal-processing electronics, information storage devices, and electronic sensors that achieve enhanced performance by reducing feature sizes below 100 nm.

Significance of scale:

100 nm:

- Minimum feature size obtainable using conventional lithography
- Significant economic barriers to continued device scaling
- The maximum feature size where quantum effects become observable

30 to 50 nm:

- Conventional Si MOSFET fails
- Quantum phenomena affect device operation
- Minimum reliable feature size for ebeam lithography

10 nm:

- Minimum lithographically achievable feature size
- Quantum effects dominate device behavior

1 to 3 nm:

- Molecular scale
- Size limit for electronic functionality

Nanoelectronics

Goals

ONR Grand Challenge:

Multifunctional Electronics for Intelligent Naval Sensors

To develop highly multifunctional nanoscale devices to their ultimate limits of high speed (100x), small size (0.01x) and low power (0.001x), that interactively combine sensing, image processing, computation, signal processing, and communications functions to achieve real-time adaptive response, all on-site, for Navy missions.

NRL nanoelectronics program ranges from long-range basic research to directed device research

Short term (1 – 5 yrs) – e.g. Nanoscale FETs
Mid term (5 – 15 yrs) – e.g. Advanced lithography
Long term (15 – 30 yrs) – e.g. Quantum coherence

SIA Roadmap

The era of Nanoelectronics is forecast to begin within 3 years

The scaling of electronic devices to increasingly smaller dimensions has resulted in:

- Faster electronics
- Lower power consumption
- Larger data handling capabilities
- More complex information processing

Year 1st Introduction	1995	1997	1999	2001	2004	2008	2011
DRAM (bits/chip)	64M	256M	1G	2G	6G	20G	45G
μP transistors/chip	5M	11M	24M	48M	135M	539M	1523M
Lithography (nm)	350	250	180	130	90	60	40
Oxide thickness (nm)	7-12	4-5	3-4	2.4-3.2	1.5-2	<1.5	<1.0
Supply Voltage (V)	3.3	2.5	1.8	1.5	1.2	0.9	0.6
Local Clock (MHz)	300	750	1250	2100	3500	7100	11000
Across Chip Clock (MHz)	300	750	1200	1600	2000	2655	3190

Nanoelectronics is the future of advanced electronics technology

Record Performance Nanometer-Scale InAs HEMTs

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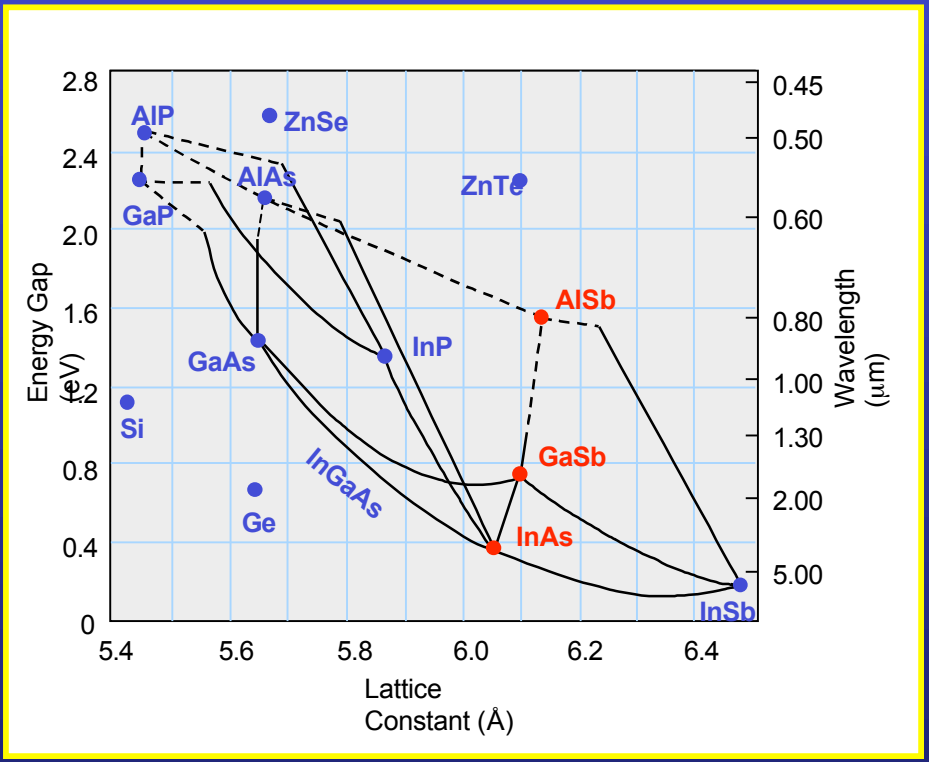
B. Bennett
W. Kruppa
R. Magno
D. Park
M.J. Yang

Sub-100 nm AlSb/InAs HEMTs

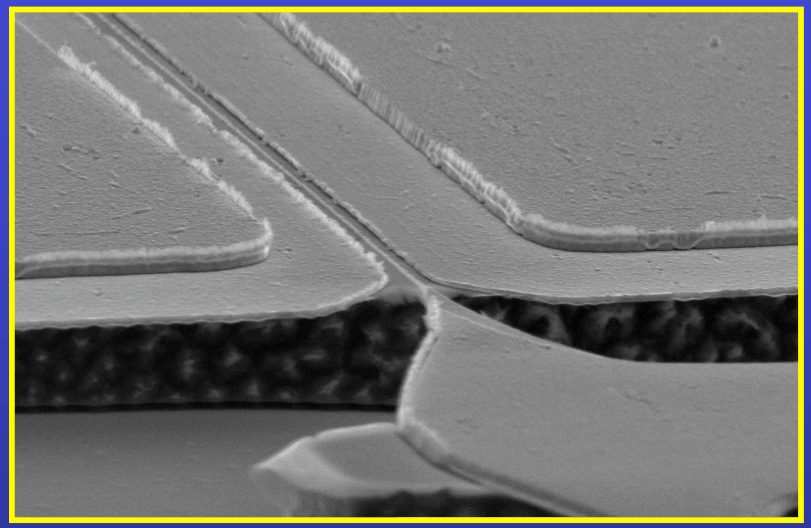


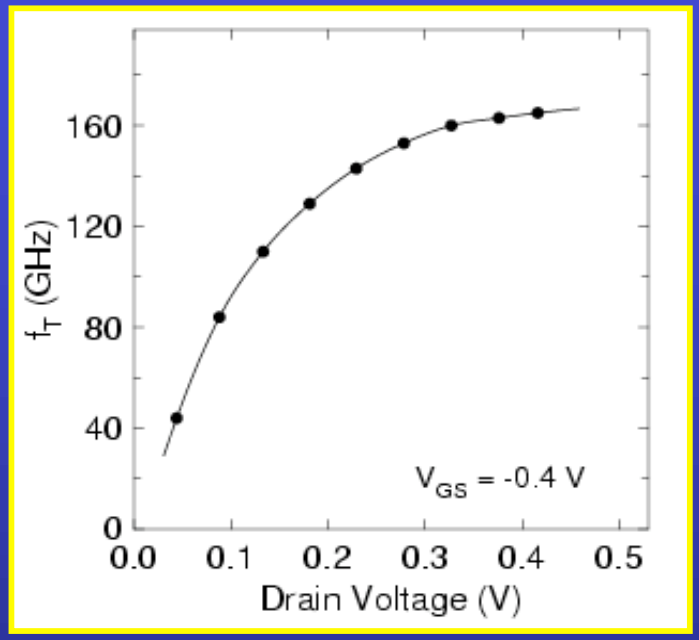
InAs/GaSb/AlSb semiconductor "family"

- **Attractive material properties for high-speed electronics**
  - High electron mobility
  - High electron velocity
  - Large conduction-band offset
  - High 2-DEG sheet-charge density

Potential for High-Speed, Low-Voltage Transistors

60 nm InAs HEMT Characteristics





Microwave Performance at V_{DS} = 0.35 V

g_m(rf) = 1 S/mm
f_T = 160 GHz
f_{max} = 80 GHz

f_T = 90 GHz at 100 mV is highest reported for a FET at this drain bias!

Ref: *J. Vac. Sci. Technol. B*, 17 (3), May 1999

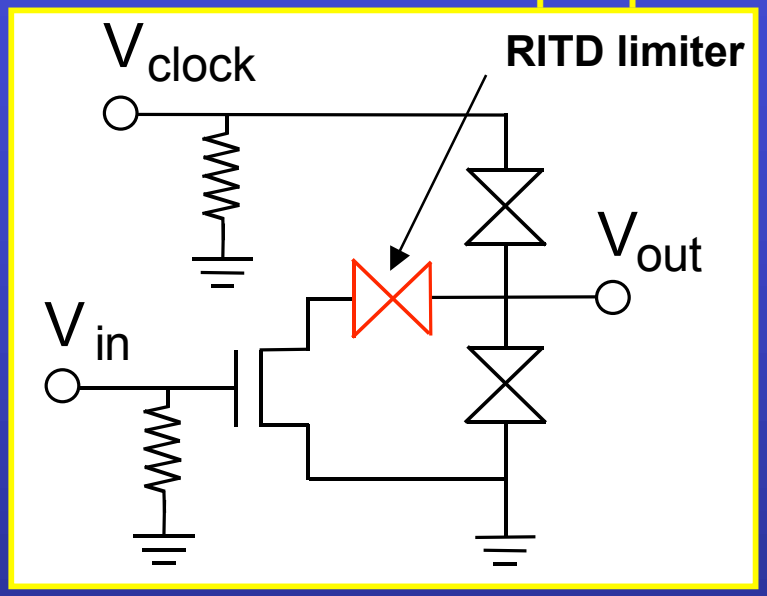
InAs HEMTs for Low-Noise Amplifiers

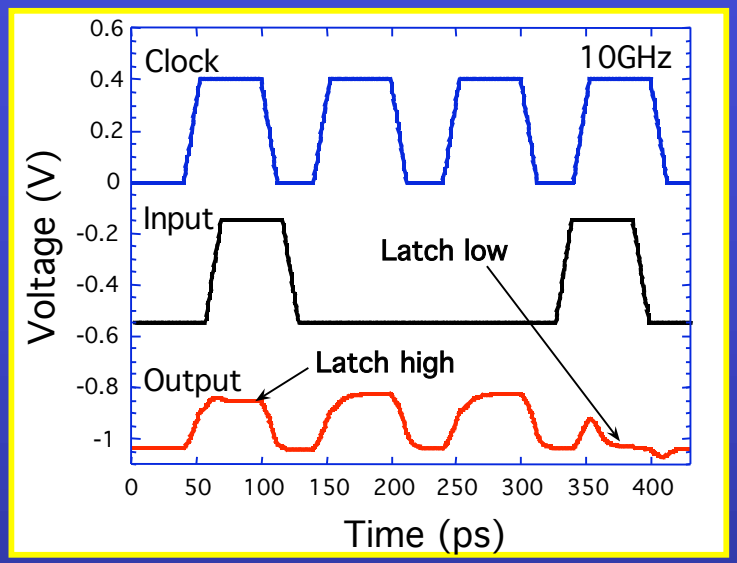
High-speed, low-power consumption electronics needed for light-weight power supplies, extension of battery lifetimes, and high data rate transmission.

- Low-noise Amplifiers
- Record low-power, high frequency performance
  - Space-based sensing and communications
  - Portable communications
  - Unihabited/Autonomous Vehicles
- Current CRADA with TRW
  - Also developing HBT

Sb-based MOBILE Circuit

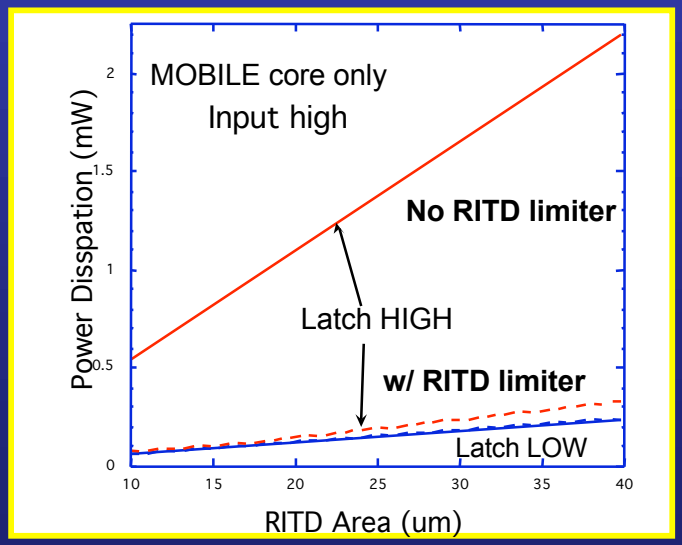
MOBILE-based flip-flop





SPICE simulations D-flip-flop

- NRL 1st to integrate InAs HEMT and GaSb RITD
- SPICE simulation of HEMT/RITD circuit predicts 5-10X lower power dissipation than comparable InP-based circuit.



Static Power

Nanometer Scale InAs/AlSb Quantum Structures

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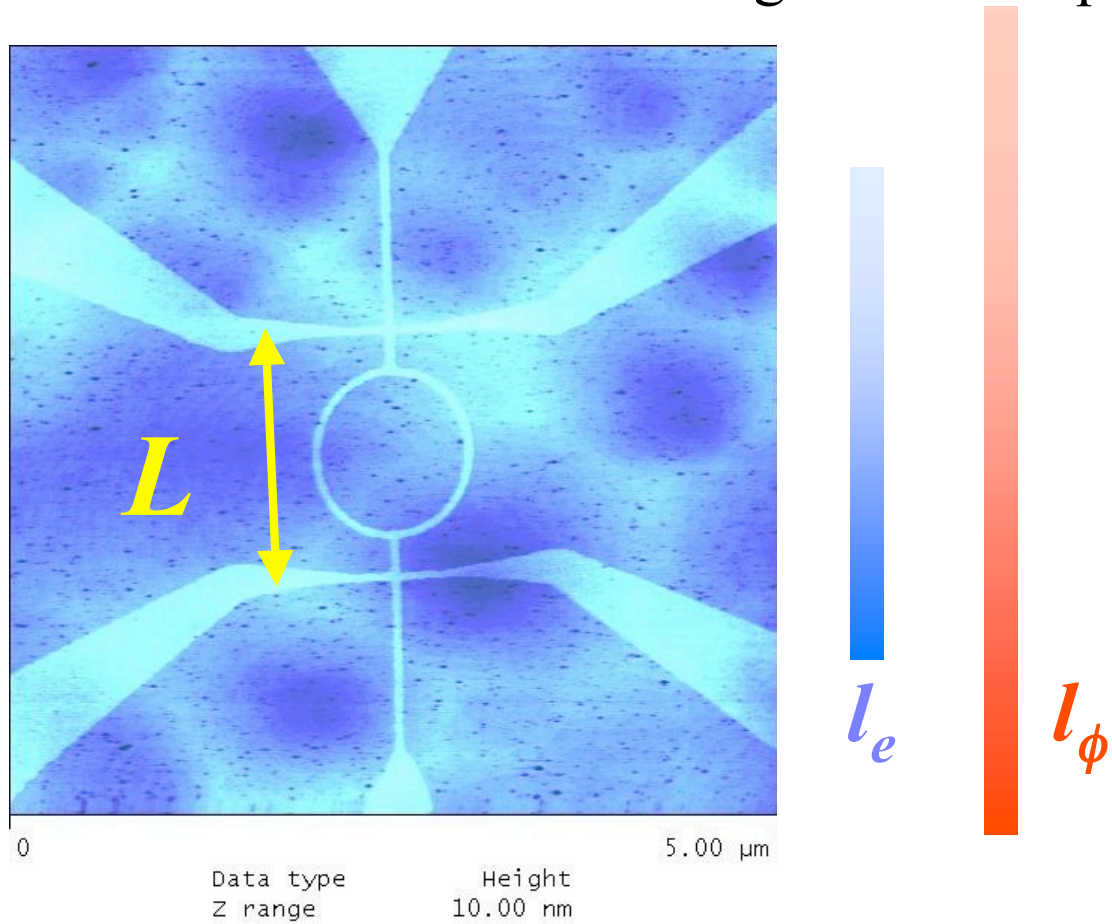
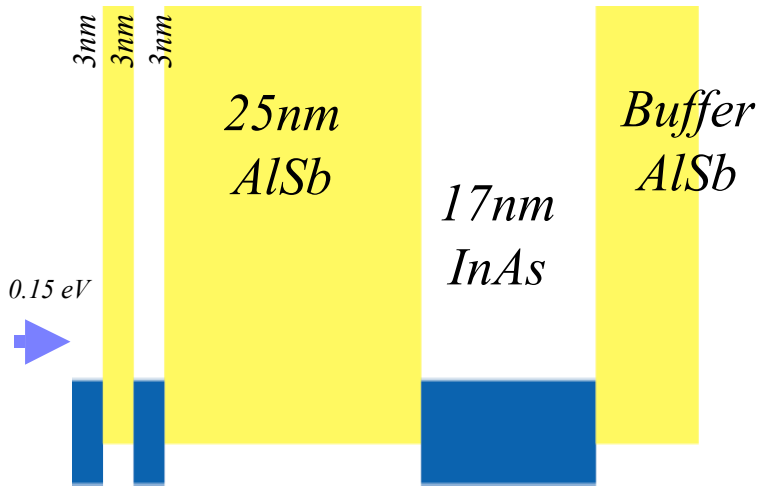
Objective: Complex quantum circuit within phase coherence length

➔ Nanometer scale wires/dots with high material quality



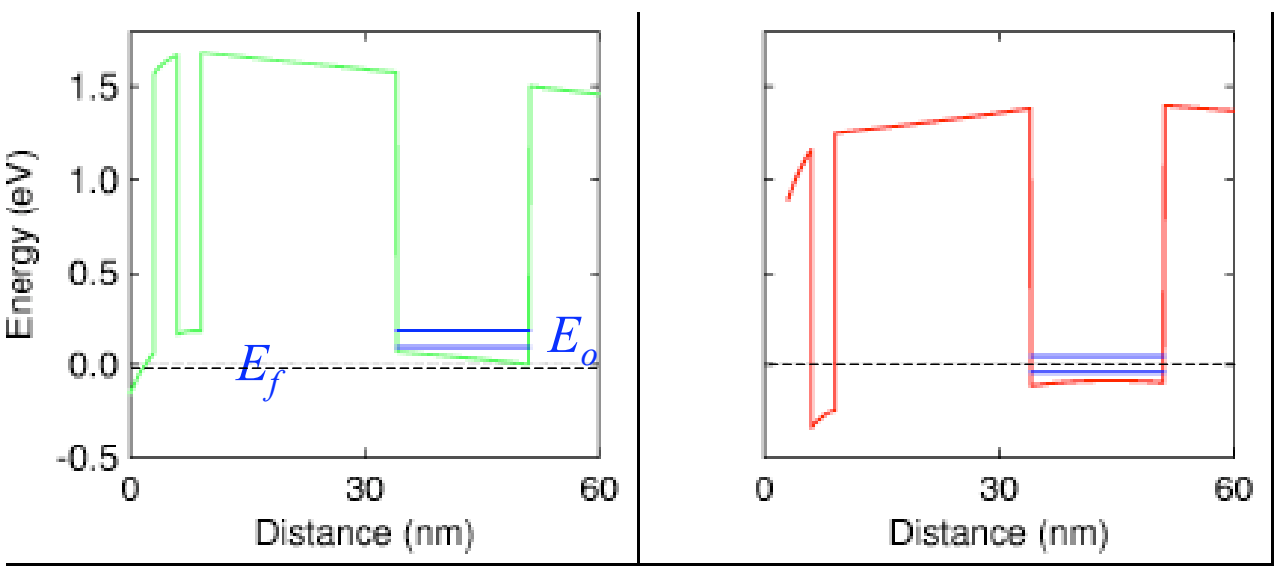
Using E_f pinning and modulation doping to control n_{2D}



*A **3nm shallow** wet-etch can provide both excellent control and no damage to the surface*

***Scheme** to define quantum wire:*

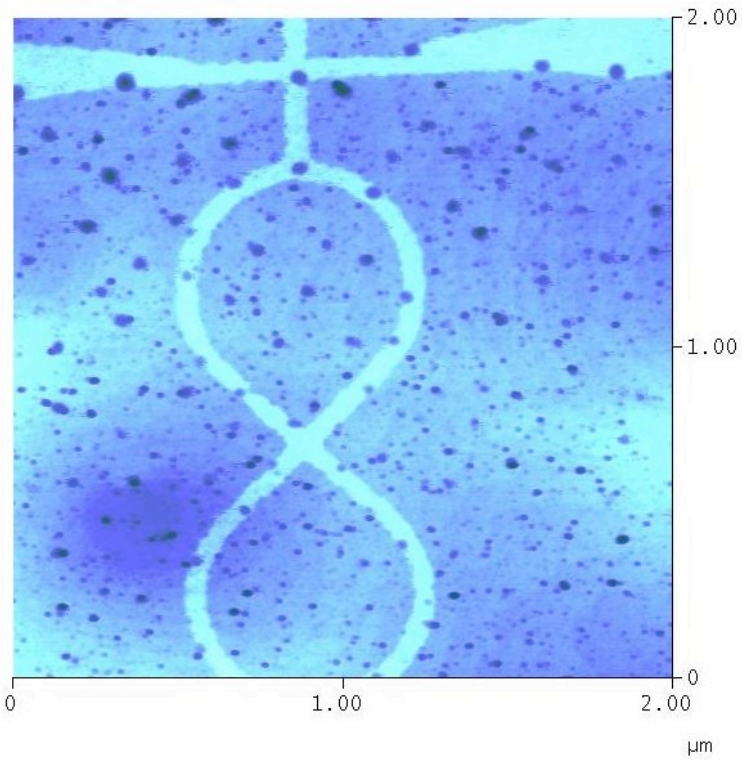
1. *As-grown is insulating*
2. *A shallow wet-etch to create a conducting channel underneath*

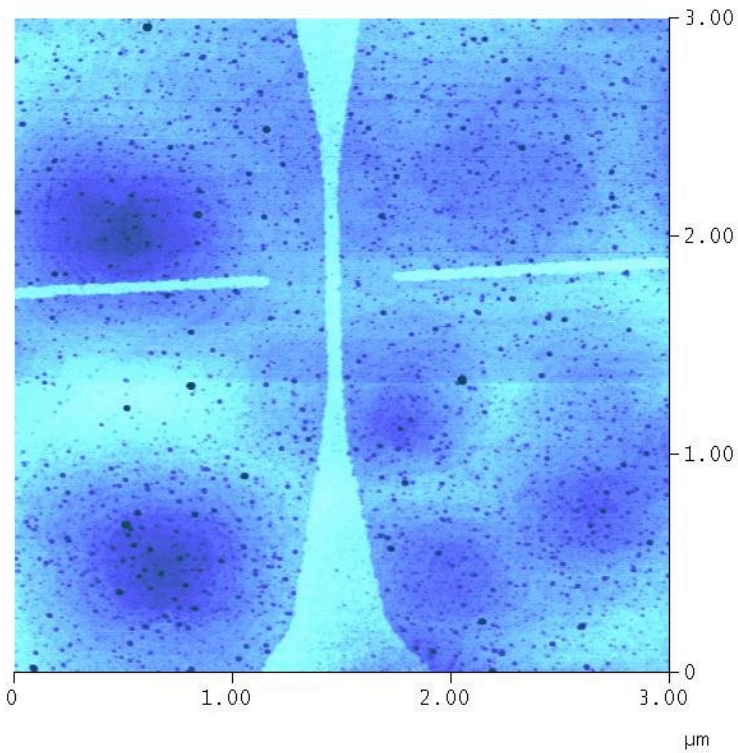


$E_f = 41$ meV
$n_{2D} = 4.92 \times 10^{11}$ cm^{-2}
$\mu = 200{,}000$ cm^2/Vs
$l_e = 2.3$ μm

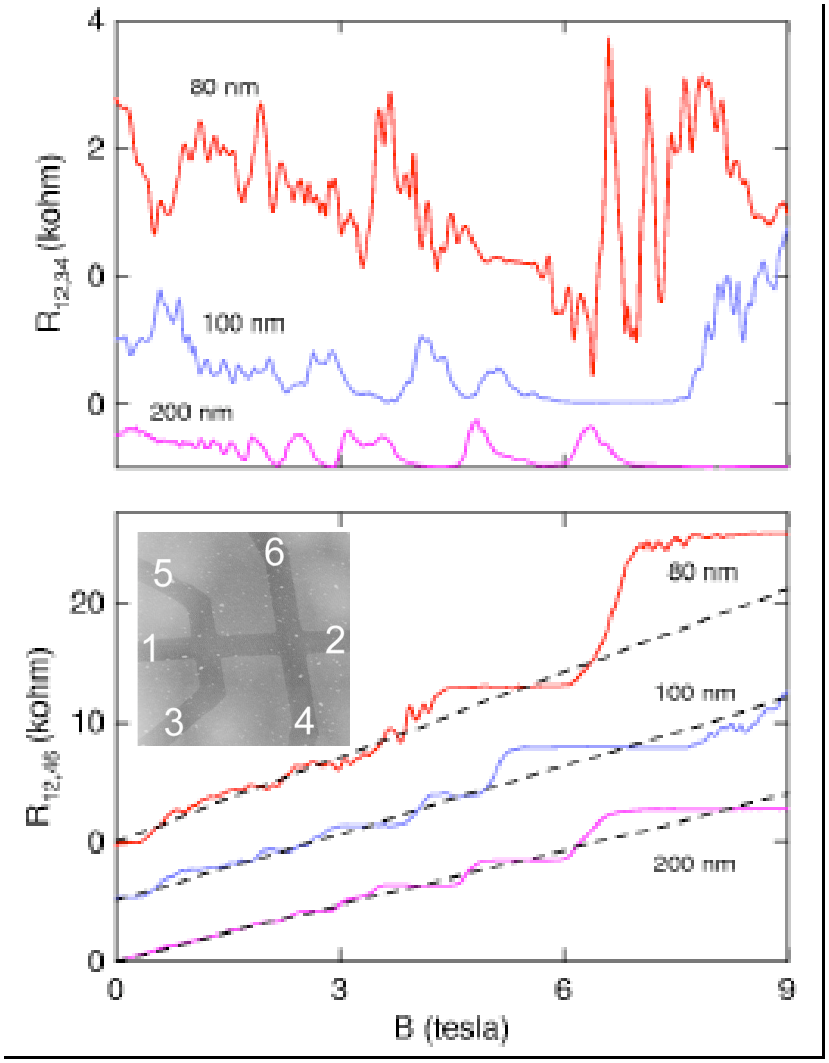
AFM Characterization

- 50 nm wire width with nm sidewall roughness
- Planer nanofabrication, simple and flexible
- Additional transport control by side gates





Magnetotransport Characterizations



The InAs nanostructures posses three important properties:

- Specular boundary scattering
  ⇒ Long elastic mean path

- Hard-wall lateral confinement potential
  ⇒ Large 1D sublevel spacing

- Conducting channel width is approximate the lithographic width
  ⇒ Width is controllable down to nm.
  ⇒ Nano devices can be placed in close proximity for quantum manipulations.

Gold Nanocluster Electronics and Sensors

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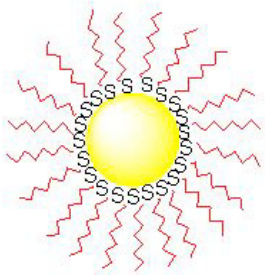
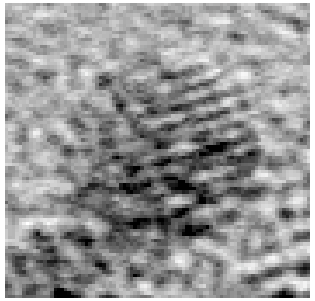
W. Kruppa
A. Snow

- Collaborative project between 3 NRL Divisions:
  - Electronics S & T Division
  - Chemistry Division
  - Center for Biomolecular S & E
- Goal: Nanocluster-based electronic devices and sensors of ultra-small size, sensitivity and power.

Gold Nanocluster Electronics

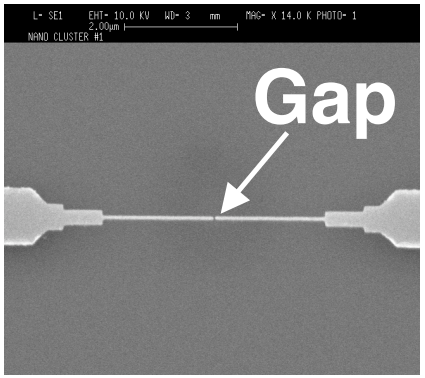
- Nanoclusters synthesized with arbitrary Au core and organic shell dimensions.

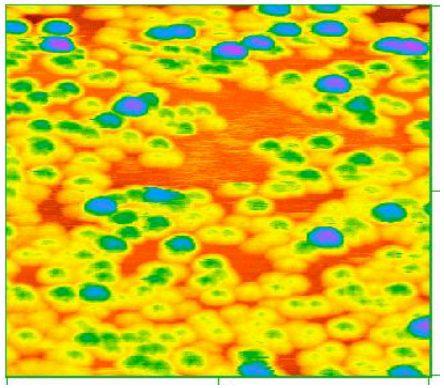




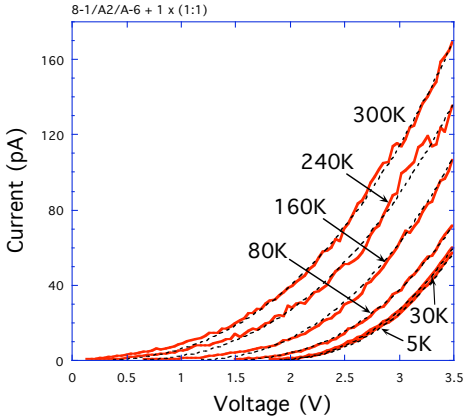
3nm

- Self-assembly onto pre-patterned substrates:

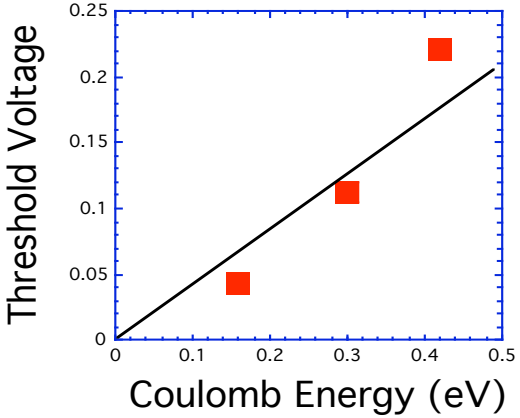




- Strongly nonlinear I-Vs due to Coulomb blockade.
  - Vary T



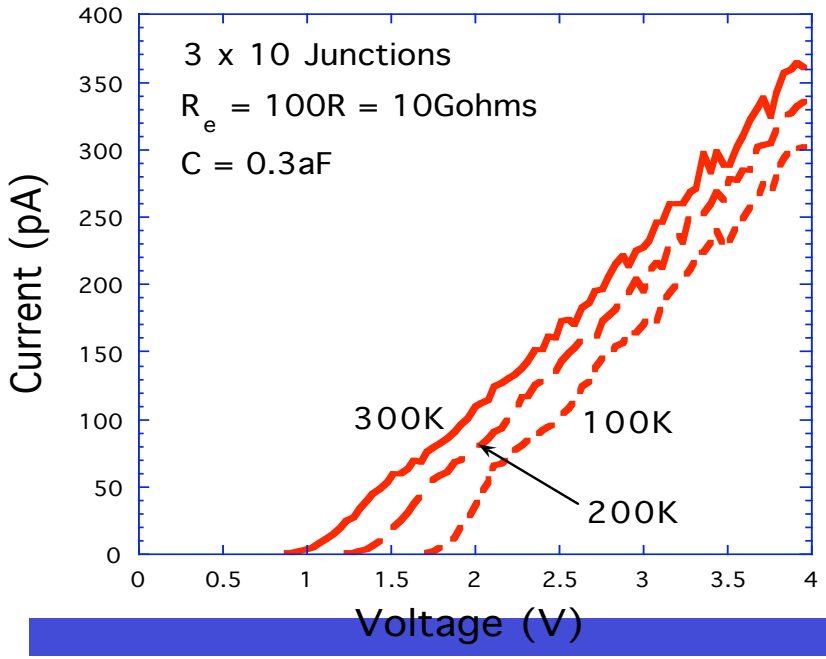
  - Vary cluster size:

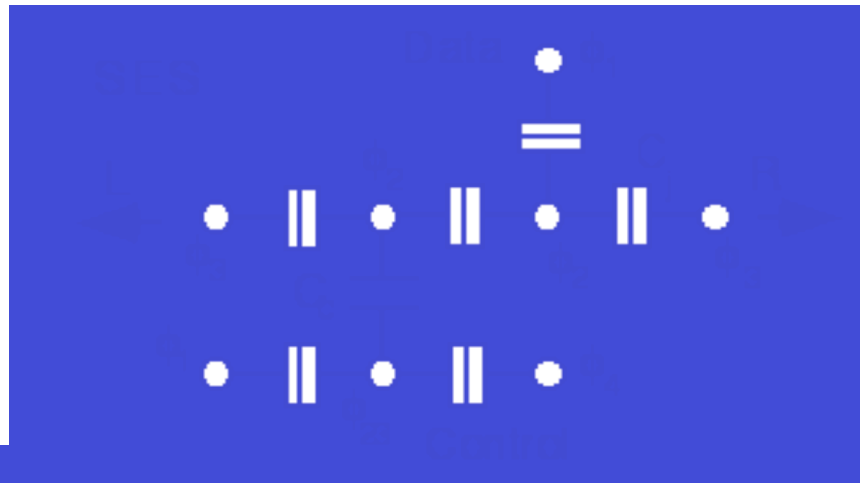


Coulomb Blockade Modeling

- Study of electron transport in complex networks of nanoclusters.
  - Include Coulomb blockade plus thermal effects and disorder.

- Study of generic Coulomb blockade circuits in the ultimate limit where single electrons represent bits.
  - Called single-electron digital circuits.
  - Main switching element --- single-electron switch:





Semiconductor Quantum Dots: Growth and Spectroscopy

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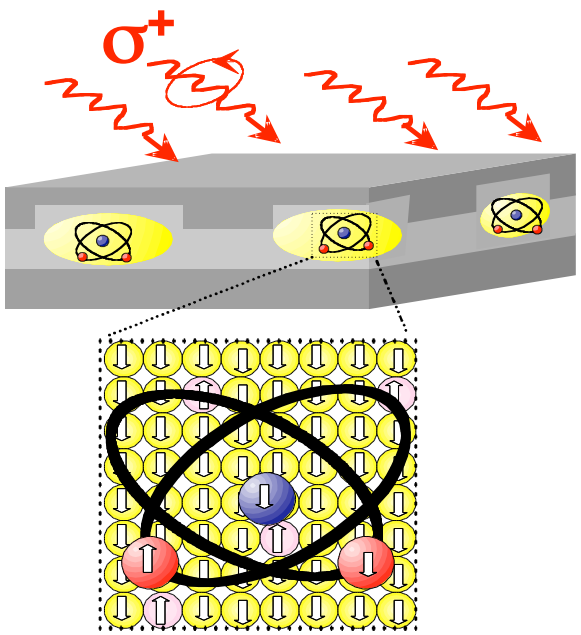


Nanostructured Electronic Materials

Molecular Beam Epitaxy

Quantum Well

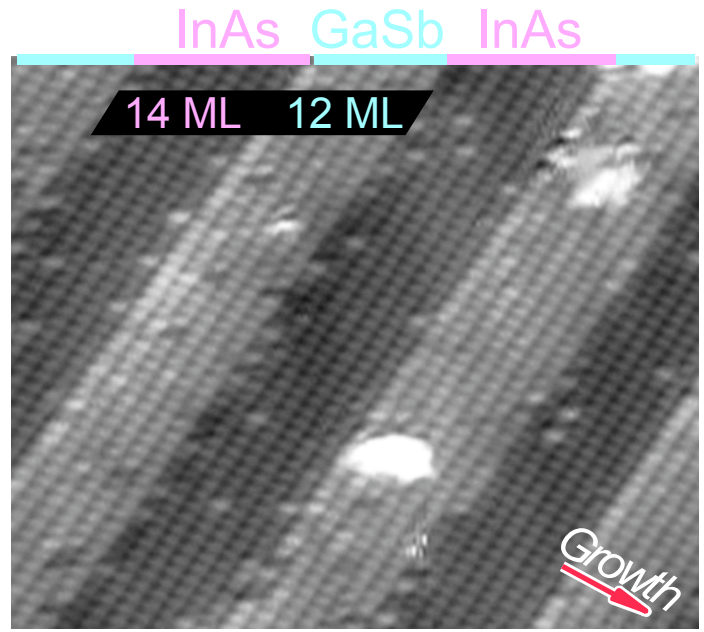
Heterojunctions

– Two dimensional

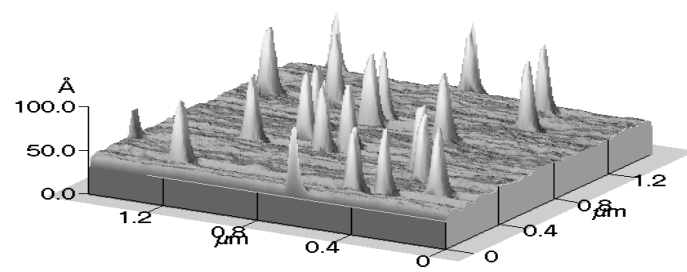
Quantum Dots

- defined on a **quantum well**
  - Etching
  - Electric fields
  - Strain fields
  - Composition (self assembly)
- Nanocrystals (colloidal chemistry)

NRL Epi-Center



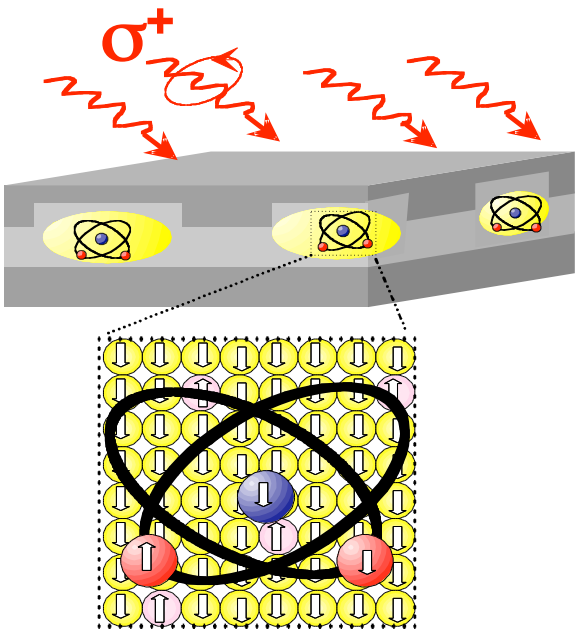
Quantum Wells (STM)

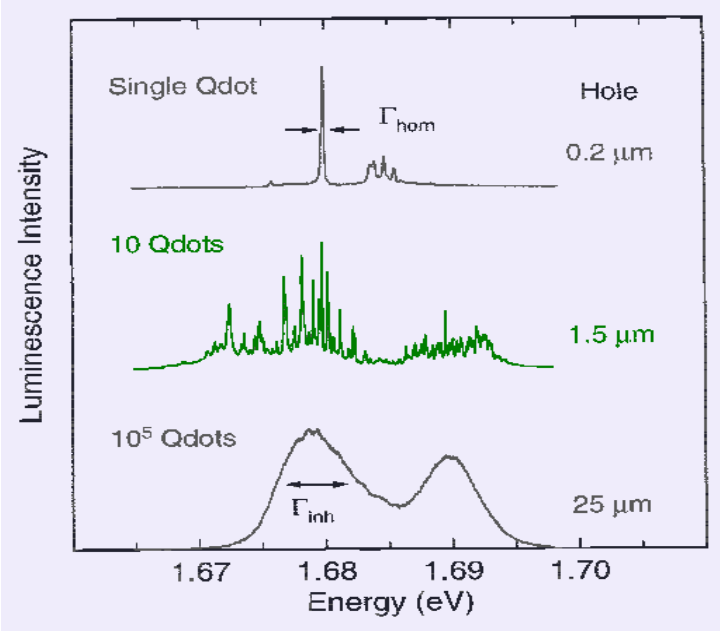


Quantum Dots

Optically Probing Single QDs

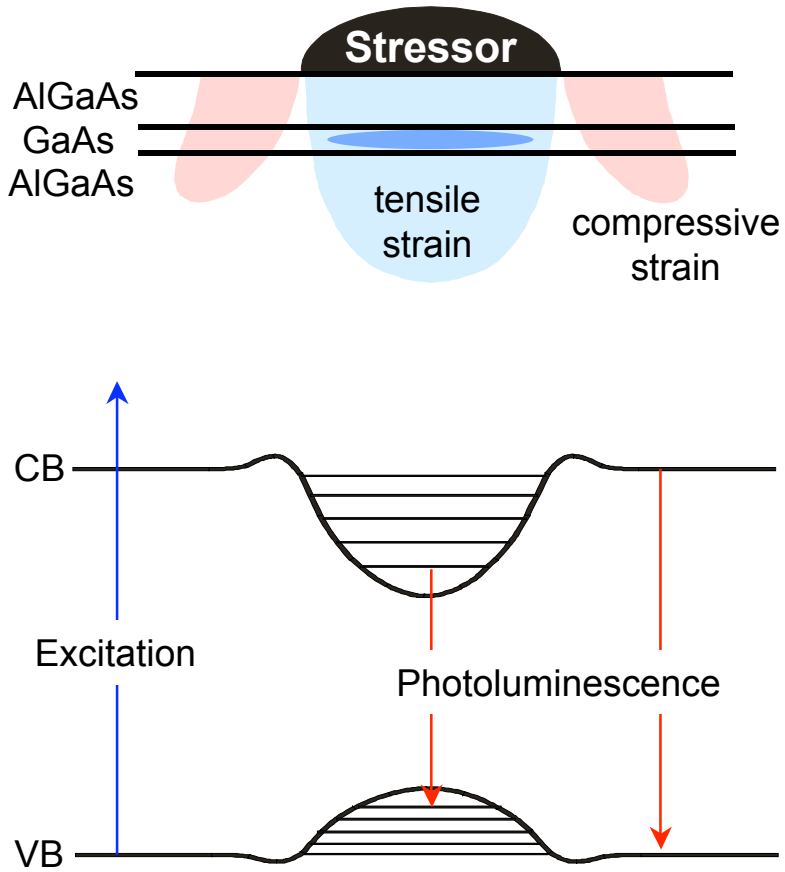
- Recent Accomplishments
  - Physics of linewidths [*Science* (1996)]
  - Fine Structure [*Phys. Rev. Lett.* (1996)]
  - NMR of Single QD [*Science* (1997)]]
  - Coherent Control [*Science* (1998)]]
  - Exciton Entanglement [*Science* (2000)]
  - Hyperfine Structure [*Phys. Rev. Lett.* (2001)
  - Rabi Flopping [*Phys. Rev. Lett.* (2001)]
  - Single Electron Spin [*Submitted for publ.*]

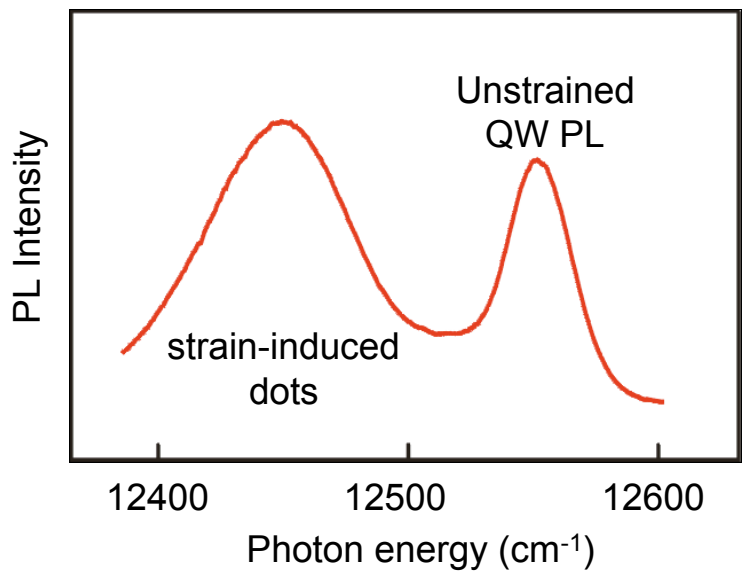




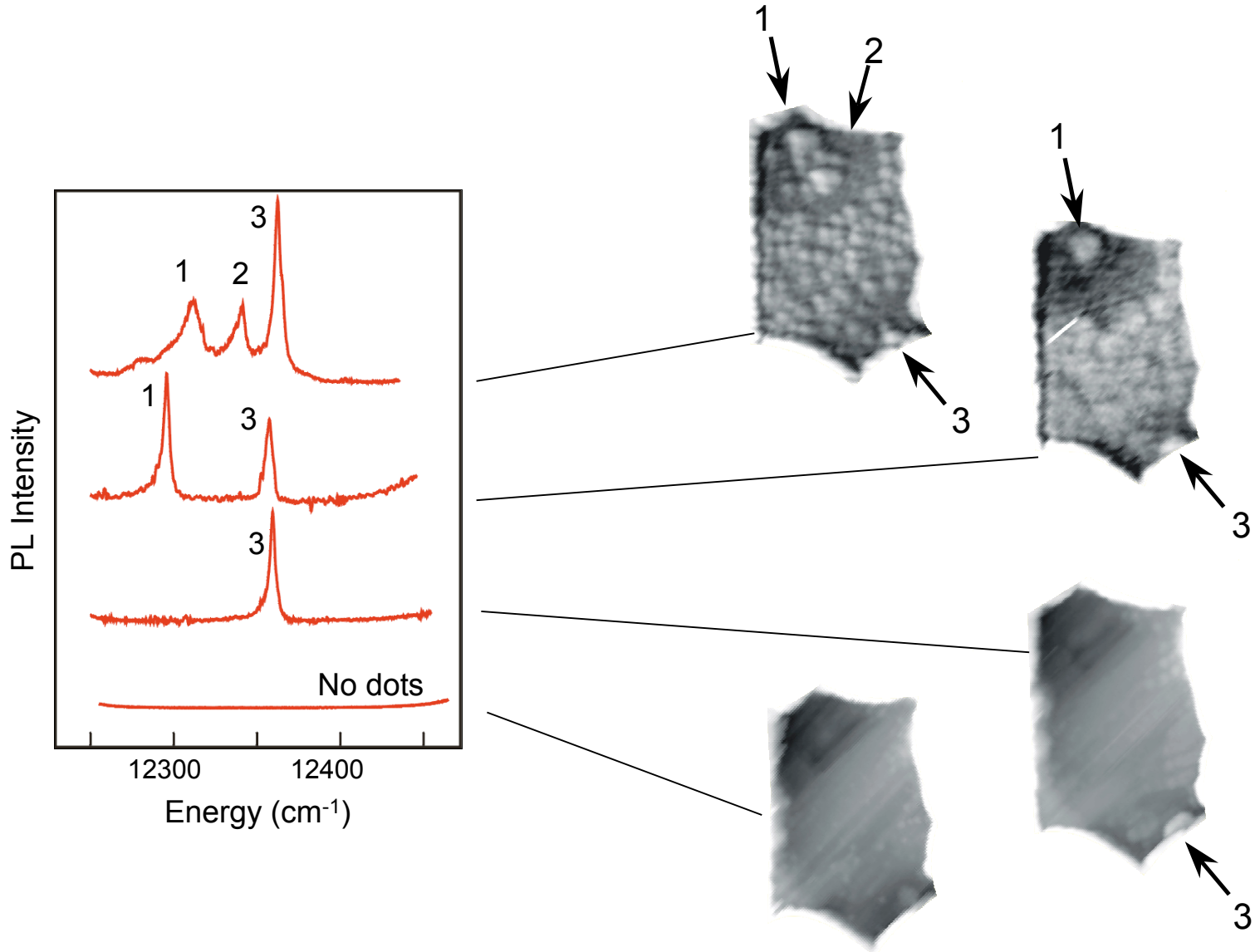
- Breaking through inhomogeneous broadening!

GaAs strain-induced quantum dots





Remove large stressors with AFM: PL lines disappear



Spin Dynamics in Semiconductors

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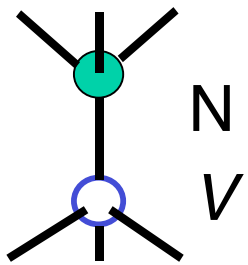
- **GOAL: Study and develop spin in semiconductors as a useful property for devices**

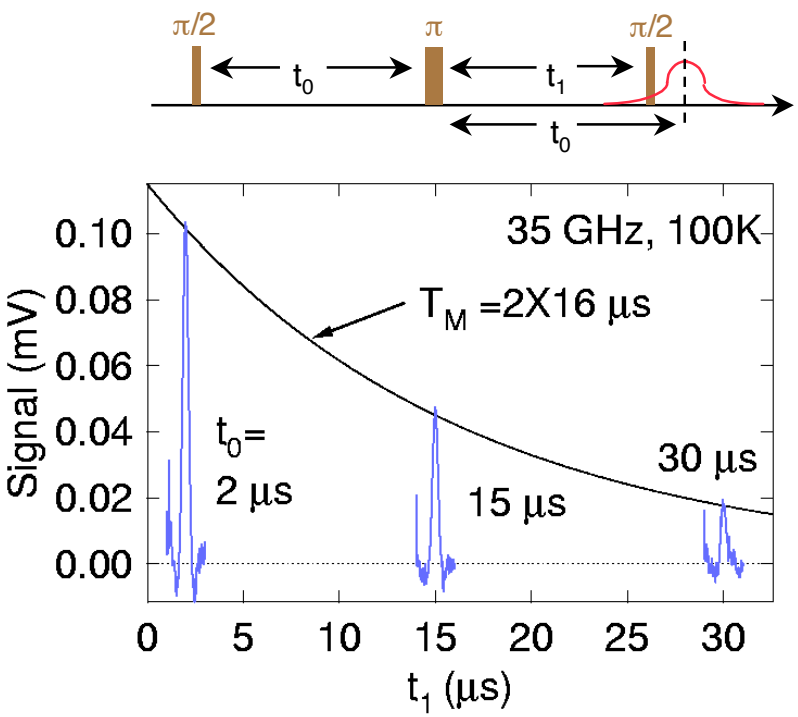
- **Active Areas**:
  - Microwave control of spin in GaAs
    J.S. Colton,* A. Bracker, J. Tischler,* T.A. Kennedy and D. Gammon
  - ZnSe:Mn nanocrystals
    D.J. Norris (NEC Princeton), Al.L. Efros, T.A. Kennedy
  - *NV-Center in diamond as a model qubit*
    F.T. Charnock,** J.S. Colton*, J.E. Butler and T.A. Kennedy

*NRL-NRC Resident Research Associate
**NRL-NRC Resident Research Associate, now at NIST Boulder

The NV-Center in Diamond as a Model Qubit



- **Nitrogen-Vacancy Pair in diamond**
  - Optical transition in near-infrared with high quantum efficiency
  - Electronic spin in the ground state



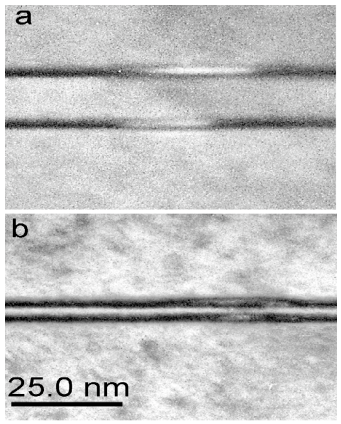
- **Optically Detected Electron Spin Echo**
  - Spin operations
    - Polarized optically
    - Controlled by μ-wave pulses
    - Detected optically
  - Phase-memory time of 32 μs in CVD diamond (LMA, Inc.)
  - Not limited to cryogenic temperatures

[Charnock and Kennedy, Phys. Rev. B 64, RC 041201 (2001)]

The NV-Center in Diamond as a Model Qubit

- **Significance**
  - New approach for Q-gates
  - Standard for solid-state qubit
    - Long phase-memory time for spin
    - High quantum efficiency for optical transition--single-defect operation possible
    - Room-temperature operation demonstrated with $T_M = 2\mu s$ (in irradiated high-pressure diamond)
- **Future Work**
  - Demonstrate long-lifetime, room-temperature operation
  - Demonstrate entanglement using ^{14}N nuclear spin
  - Demonstrate Grover's quantum search algorithm with a two-qubit solid-state quantum computer

THEORY OF SEMICONDUCTOR NANOSTRUCTURES



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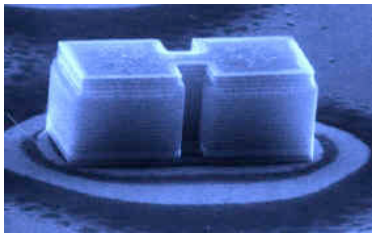


NRL participants:

- Yu. Lyanda-Geller, visiting scientist
- L. M. Woods, NRC Research Associate

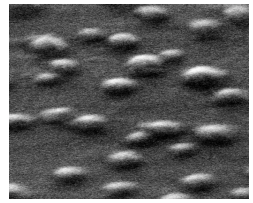
collaborators:

- M. Bayer, A. Forchel, University of Wuerzburg, Germany
- D. A. Broido, Boston College
- P. A. Knipp, Christopher Newport College
- S. Rudin, Army Research Laboratory

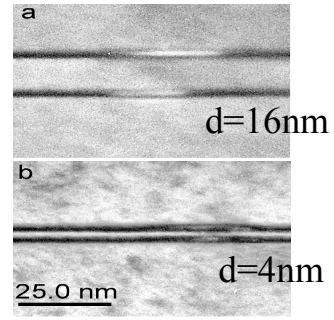
COUPLED QUANTUM DOTS

- coupling between dots critical need for quantum gates
- pairs of high quality Stranski-Krastanov quantum dots studied theoretically with expt
- demonstrate qu-bit entanglement

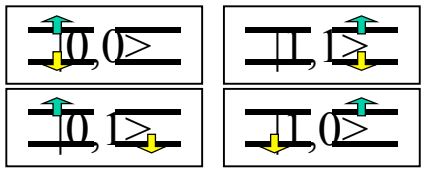
dots



coupled dots

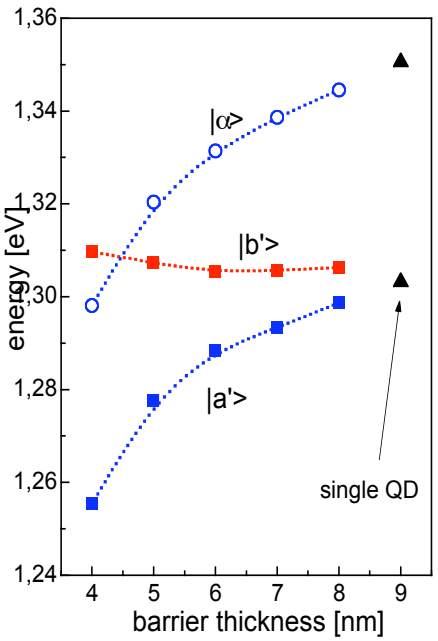


exciton qubits

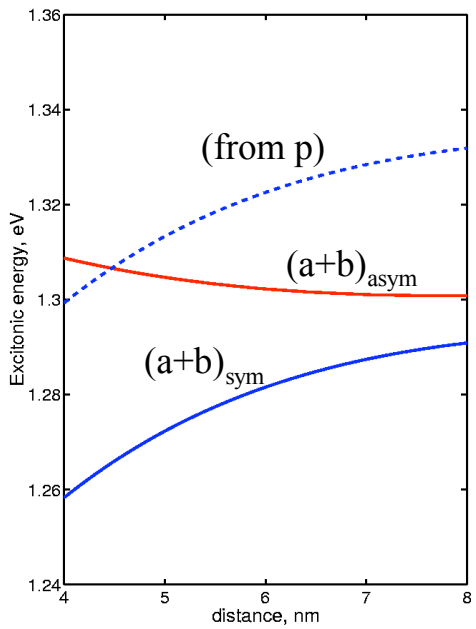


MAGNETIC ANTICROSSINGS DEMONSTRATE COUPLING

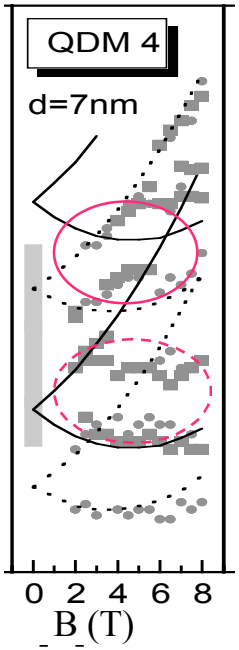
photoluminescence



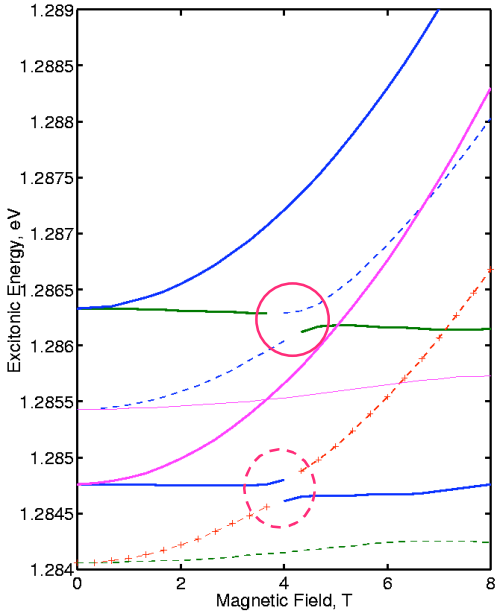
calculations



expt

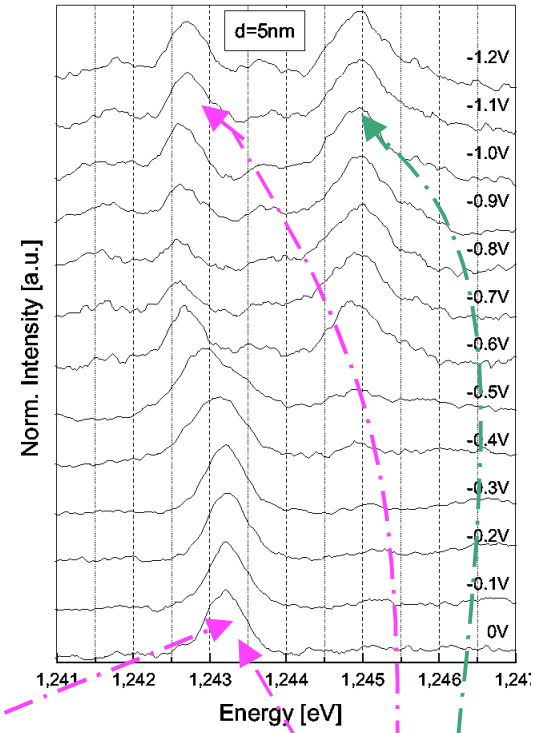


calculations

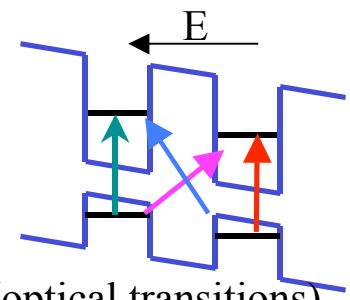


CONTROL ENTANGLEMENT WITH FIELDS

- control of entanglement critical need for quantum gates
- demonstrate electric field controls entanglement of exciton qu-bits
- joint theoretical work with expt.
- optically dark states have potential for storage

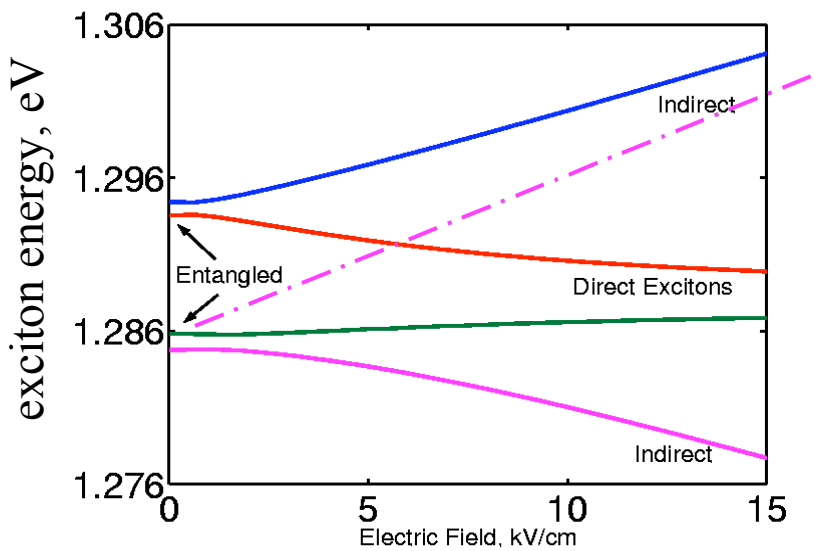


experiment

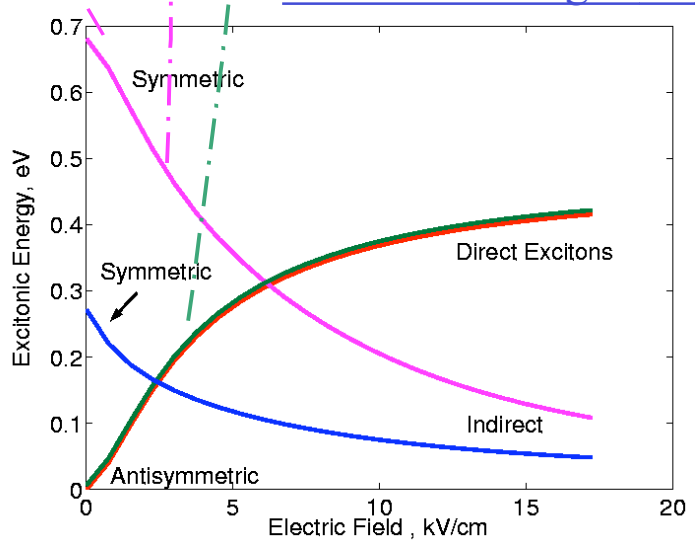


(optical transitions)

spectra vs electric field



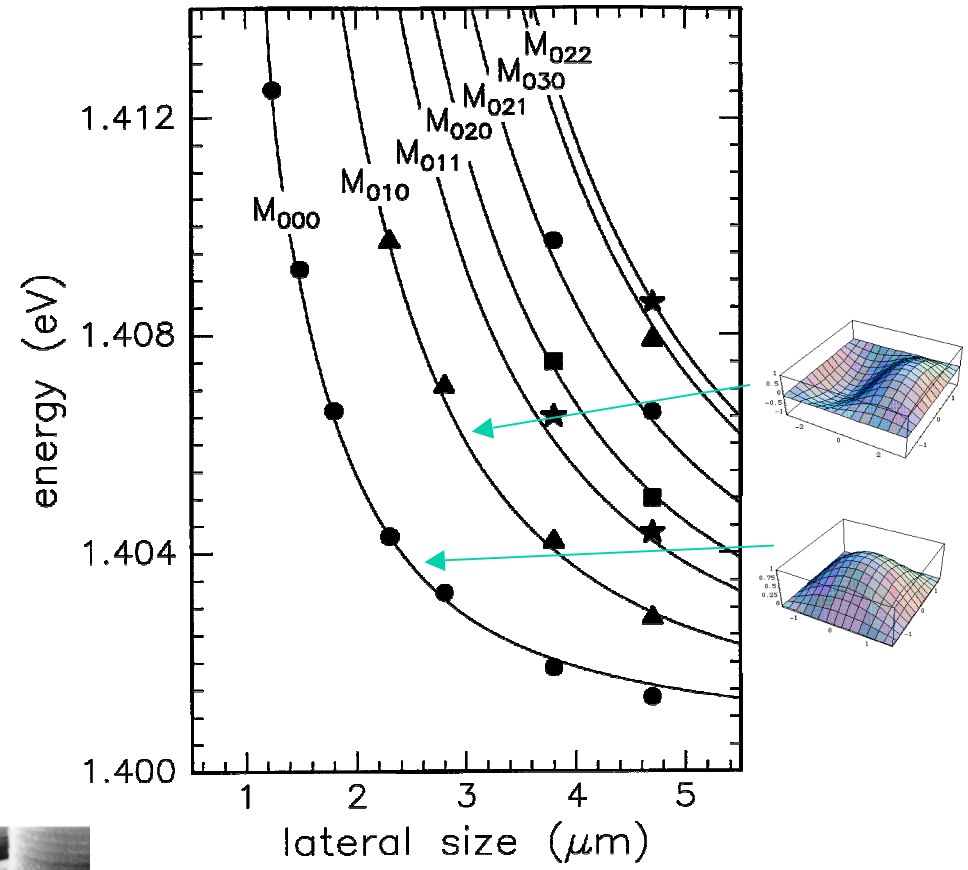
oscillator strength vs field



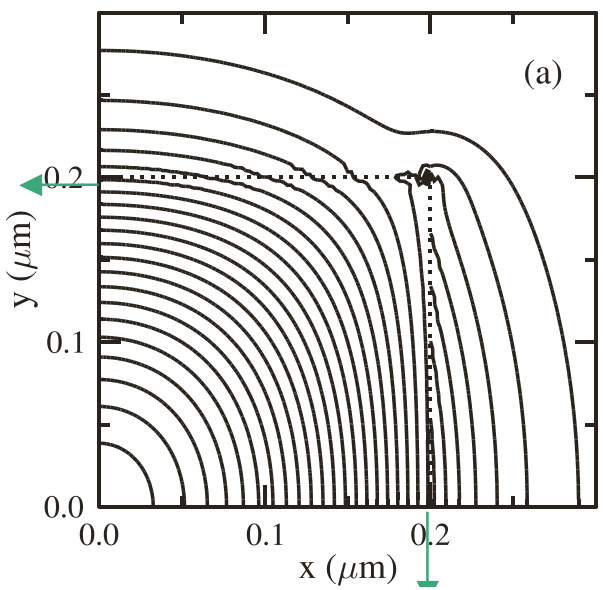
OPTICAL MICROCAVITIES

- optical microcavities of much current interest for cavity-QED in optical regime, e.g. control spontaneous emission (microlasers, LED's, etc) and fast coupling in quantum computation
- joint theoretical/experimental work on lithographic GaAlAs cavities with InGaAs quantum wells
- demonstrated fully confined modes in cavities, control of modes in coupled cavities and photon band gaps in chains

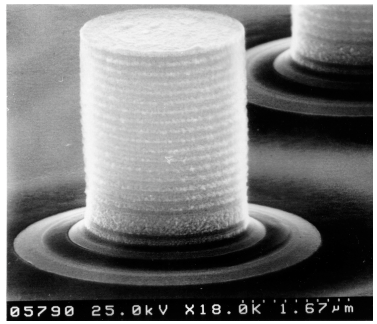
photon 'confinement energy'



calculations



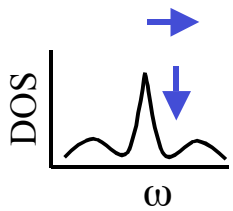
structures



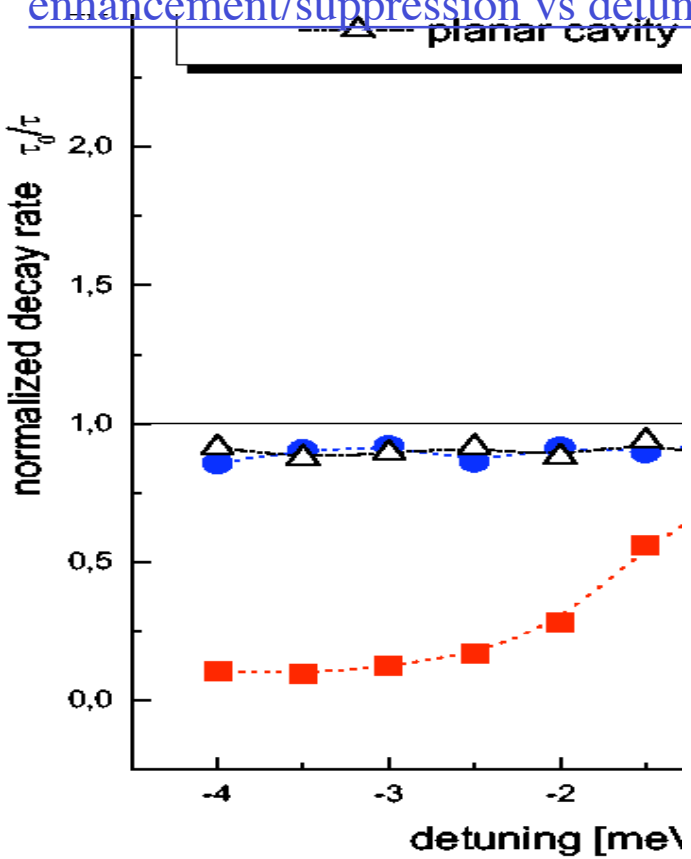
Phys. Rev. Lett. **78**, 378 (1997)
Phys. Rev. Lett. **81**, 2582 (1998)
Phys. Rev. Lett. **83**, 5374 (1999)
Phys. Rev. Lett. **86**, 3168, (2001)

CONTROL OF EMISSION

- on/off resonance emission enhanced/suppressed through control of photon density of states in cavity
- of importance in LED's, lasers, excitonic quantum gates



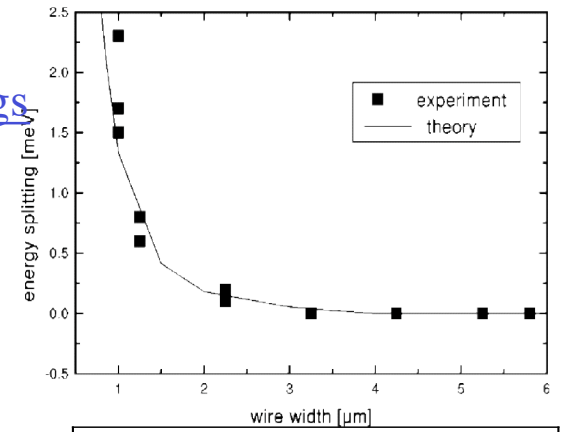
enhancement/suppression vs detuning



PHOTON QU-BITS

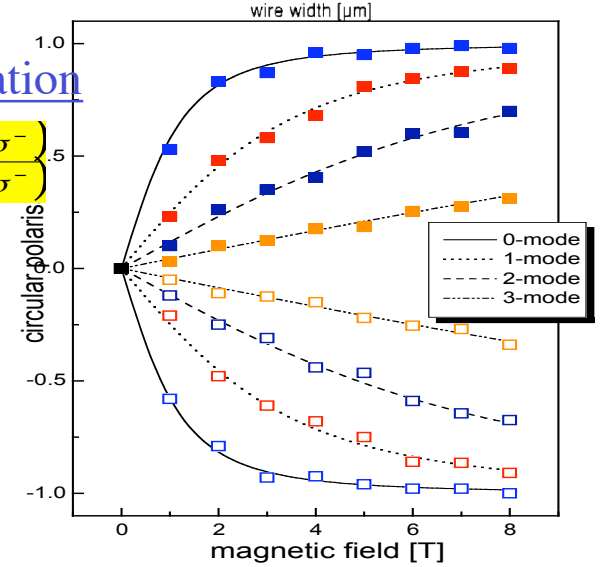
- photon polarization qu-bits of interest for secure communications, encryption
- demonstrated control of polarization and splittings with geometry and magnetic field

splittings



polarization

$$P = \frac{I(\sigma^+) - I(\sigma^-)}{I(\sigma^+) + I(\sigma^-)}$$



Nanofabrication: Breaking the 10 nm Barrier

Eric Snow
Snow@blochl.nrl.navy.mil
Paul Campbell
James Novak

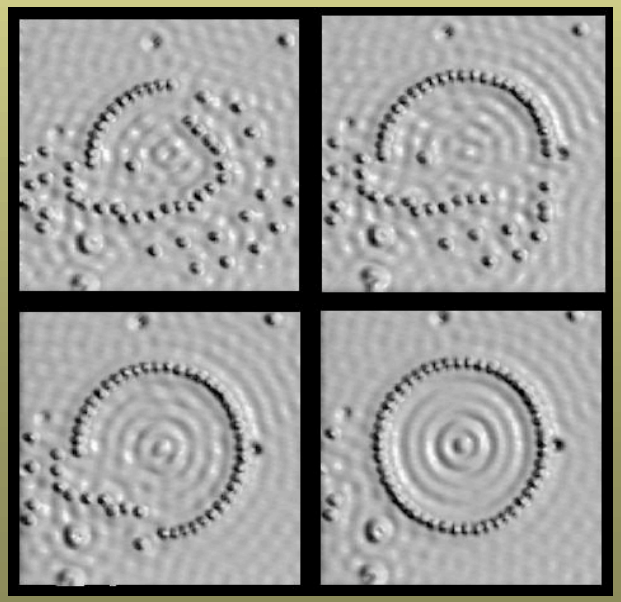
Nanolithography Tools

Conventional lithography

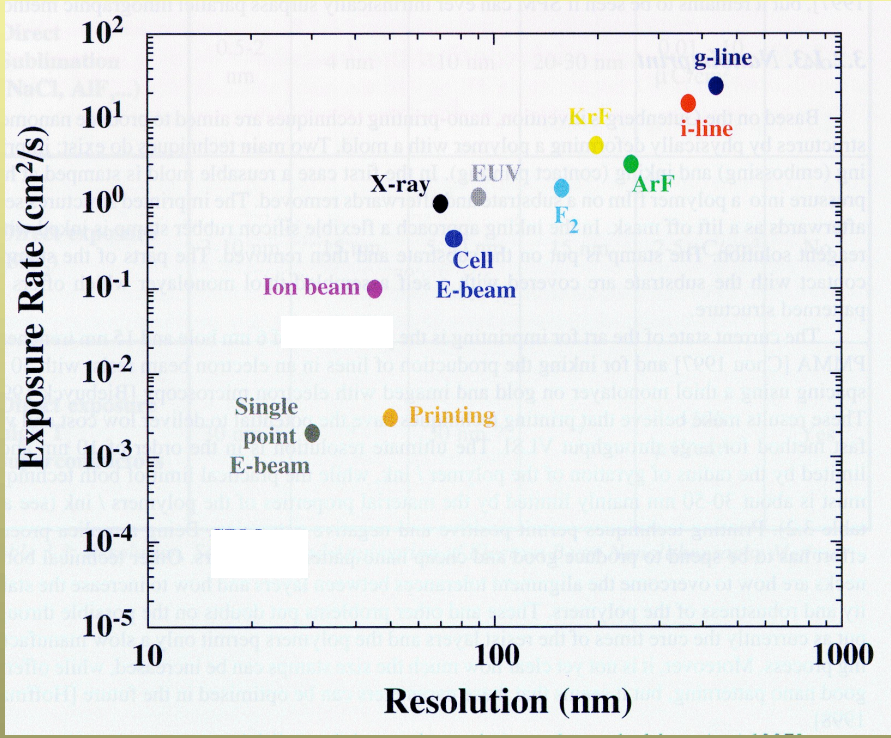
- Exposure rates drop rapidly below 100 nm
- No existing lithography for 10 nm and below

Scanned Probe Lithography

- Demonstrated atomic-scale resolution
- Equivalent exposure rate ~ 10^{-18} cm^2/s, i.e. academic curiosity
- Atomic manipulation intrinsically slow
- Are there more practical exposure and pattern transfer processes?



Don Eigler, IBM

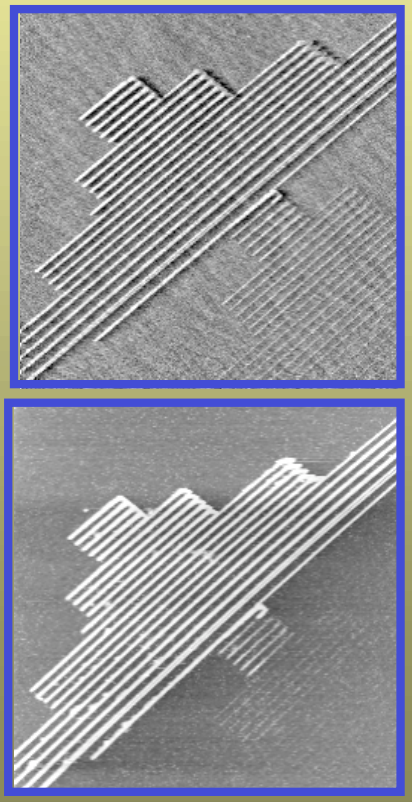


Throughput of various lithographic techniques

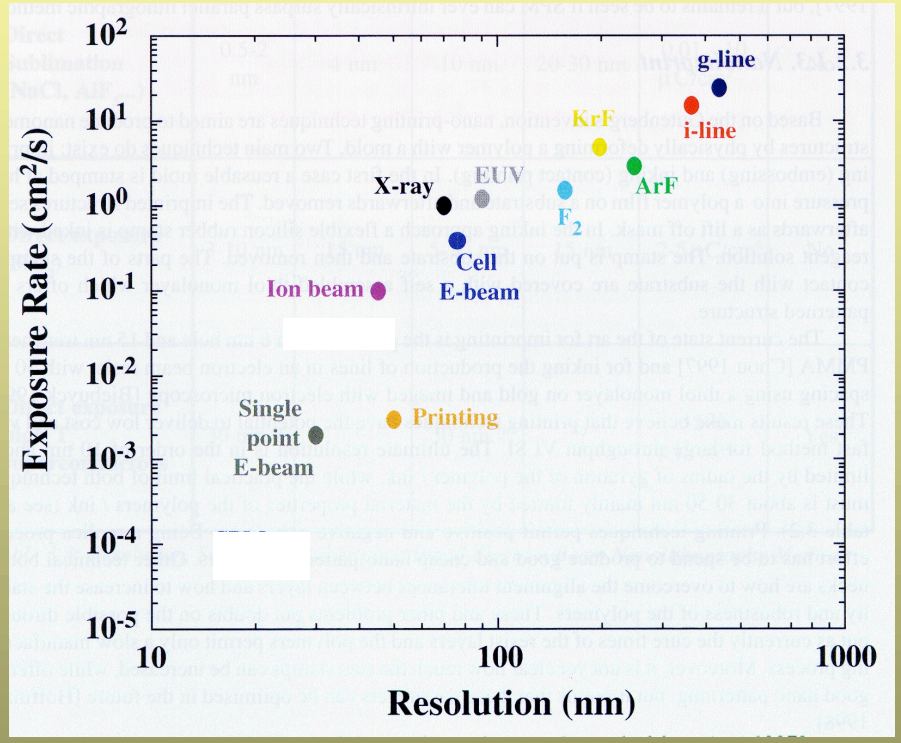
Nanolithography Tools

Scanned Probe Lithography

- 1993 – We demonstrated more practical exposure and pattern transfer process
- Equivalent exposure rate ~ 10^{-9} cm^2/s with 30 nm feature size
- Many device demonstrations
- Useful laboratory tool



Patterning Si nanostructures



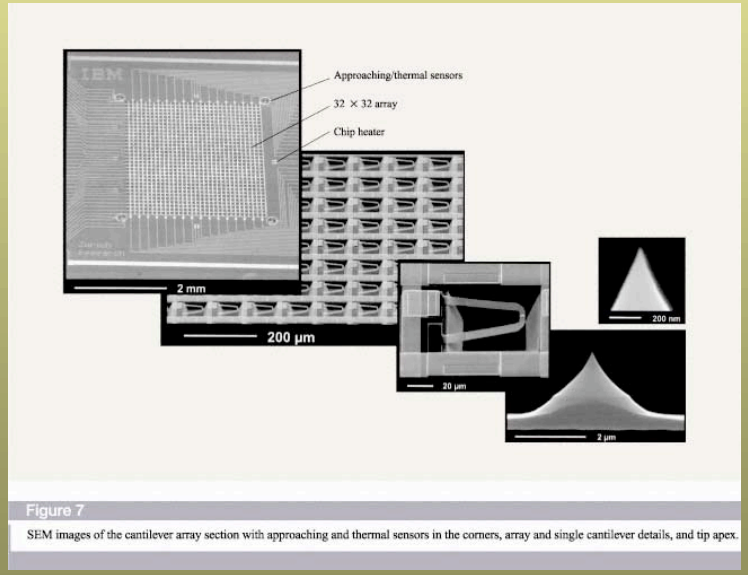
Throughput of various lithographic techniques

SPL

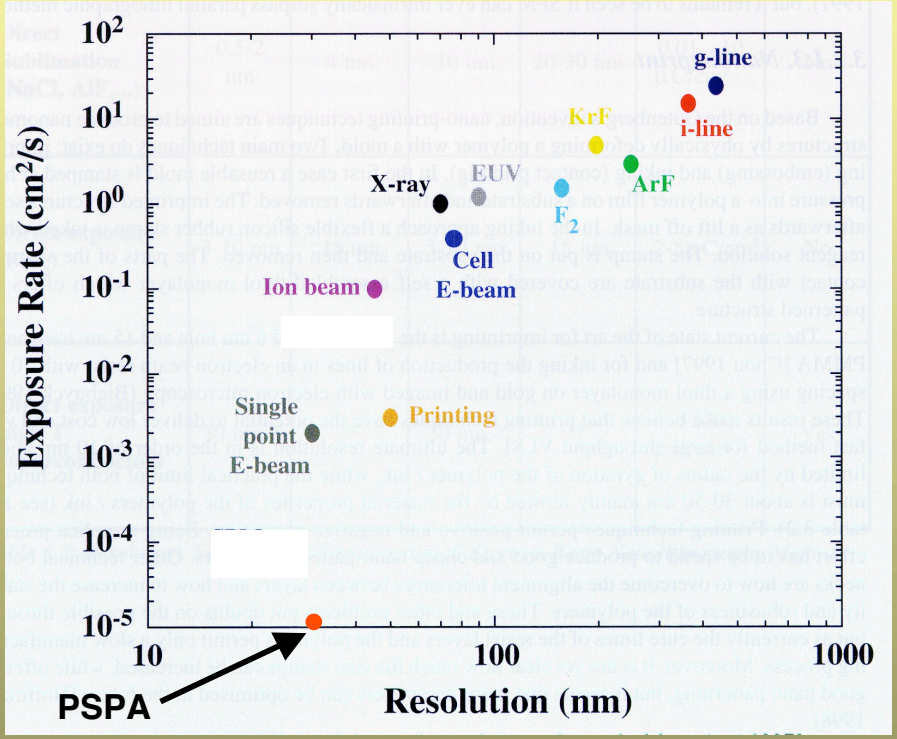
Nanolithography Tools

Parallel Arrays of Scanned Probes

- Stanford, IBM Zurich, HP, Northwestern Univ.
- Demonstrated ~ 10^3 tips operating in parallel
- Goal 10^4 tips
- Equivalent exposure rate ~ 10^{-5} cm^2/s



"Millipede", IBM Zurich

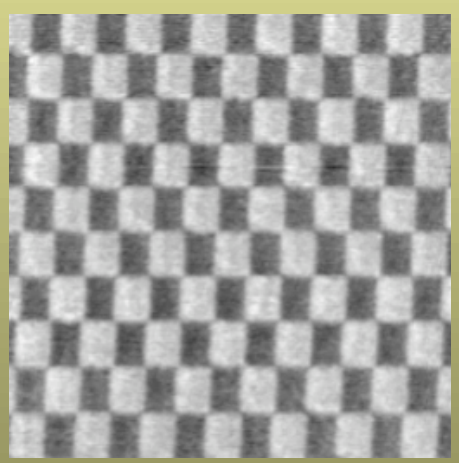


Throughput of various lithographic techniques

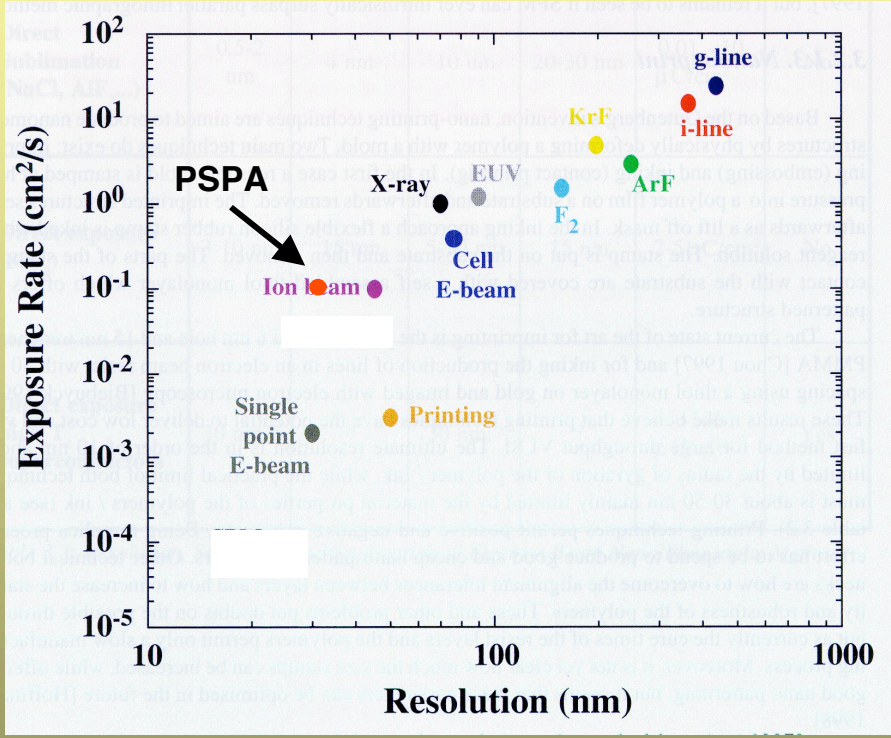
Nanolithography Tools

Fast Exposures

- We developed understanding of rate-limiting step in exposure process
- Increased exposure rate 4 orders of magnitude
- Equivalent exposure rate ~ 10^{-1} cm^2/s using parallel scanned probe array
- Many technological hurdles remain to be solved



Pattern written by selectively exposing a 128 x 128 array of pixels with –12 V, 1 μs bias pulses.



Throughput of various lithographic techniques

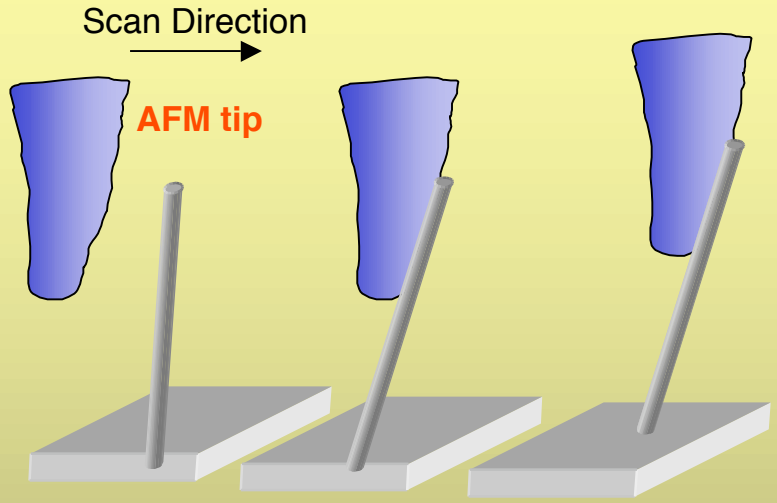
Sub-10 nm Lithography

Carbon nanotube tips (< 2 nm dia.) are ideal for fabricating sub-10 nm features in air ambient environment:

- Small tip diameter
- Mechanically and electrically durable
- Electrically conducting.

10 nm SiOx Lines on Si: Dai, Stanford

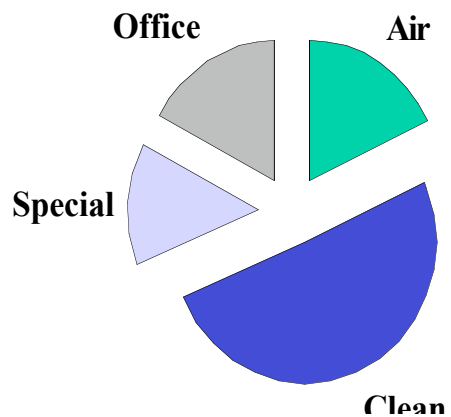
- Demonstrated < 10 nm feature size
- Current effort:
  - Improved tip preparation
  - 3 to 5 nm minimum feature size
- Ultimate goal: Fabrication in the molecular size regime

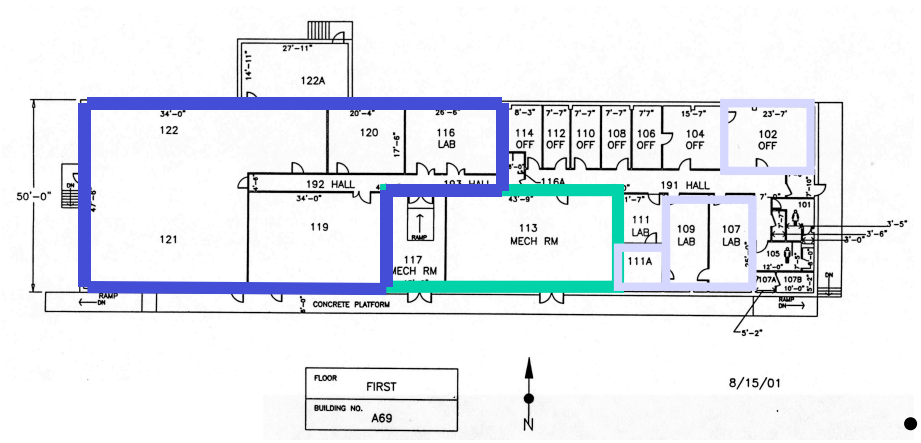


Hafner, et al, JPC-B 105 (2001)

Nanotubes grown directly on arrays of AFM tips

NPF: Key Equipment

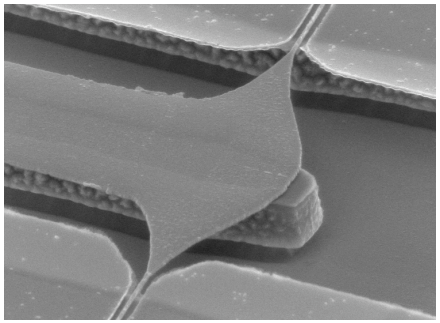
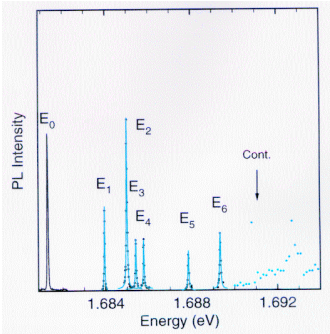
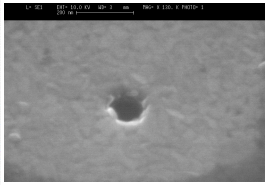
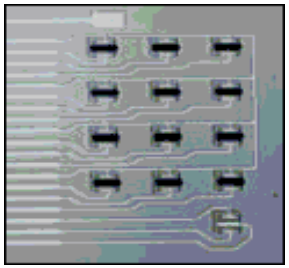
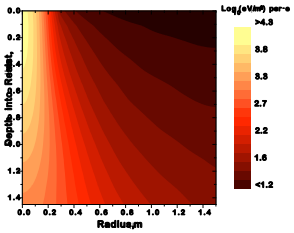




- 2 e-Beam Nanowriters
- Reactive Ion Etcher
- Ion Miller
- *ICP Etcher*
- Variable Voltage FESEM
- 2 Critical Point Dryers
- 4 Point Probe Station
- 4 CAD Stations

- Furnace Suite: 6 tubes
- 2 CVD Deposition Systems
- 4 Vacuum Evaporation Systems
- *DUV Stepper*
- 4 Contact Printers, DUV
- Profilometer
- Wet Processing Stations
- 2 Saws and 3 Bonders
- Metal Plating Baths

NPF: Impact



- InAs FETs, ESTD
  - World record low voltage high frequency performance
- Nanolithograpghy on Curved Surfaces, NPF/CBSME
- Deep sub-Micron Membrane Masks
- NanoApertures, ESTD
  - Single quantum dot spectroscopy
- Sensors, MSTD
- Low Density Targets, PPD
- Arrayed BioFET Sensors, CBMSE/ESTD
  - Label-free Bio Detection
- GaN Device Research, ESTD
- Limits of Lithography, NPF
- SEM Standards, NIST
- Non-Volatile Memory, MSTD