

Frequency Agile Target Array Controller

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Background: NRL has developed and operates a large number of unique test facilities to conduct its research. One such facility, the Central Target Simulator (CTS), was designed to conduct real-time hardware-in-the-loop (HIL) simulations over the 8-18 GHz frequency range to evaluate and improve U.S. Navy electronic warfare (EW) systems, technologies, and techniques for countering the antiship missile (ASM) threat. The CTS uses actual radio frequency (RF) system hardware (e.g., missile seekers, EW equipment) and mathematically derived computer models to perform a realistic electromagnetic and physically dynamic simulation of the various elements of naval tactical engagements.

Many of the more advanced missiles that now threaten U.S. Navy ships use radar seekers with frequency agile capabilities to acquire and track their targets. In addition to rapidly reducing (decorrelating) the effects of sea clutter, frequency agile radars are also better able to resist the effects of noise and interference. For instance, noise jamming (the intentional emission of RF energy at same transmit frequency) is a common method for interfering with radar operation. However, if the missile radar is frequency agile, effective jamming becomes more difficult to achieve because of the need to either spread RF energy over the full agility bandwidth or make an intelligent prediction of the next incoming transmitted frequency (which can be very difficult in a tactical scenario). Accordingly, NRL is actively pursuing the development of effective countermeasure technologies for such threat systems, and the CTS facility was recently upgraded to generate RF target returns that accurately follow the pulse-to-pulse frequency agile transmissions for such seekers.

Frequency Agile Upgrade: This CTS upgrade has three major components. The first is the Frequency Agile Signal Processor (FASP), which is an instantaneous frequency measurement (IFM) system. On a pulse-by-pulse basis, the FASP rapidly measures the seeker's transmit frequency and tunes a fast synthesizer to this value so that the simulated returns are correctly radiated. The second component of the upgrade is a new calibration system. The calibration system measures the amplitude and phase of the RF paths and the associated components (attenuators, phase shifters, and solid state and tube amplifiers) over a 1.0 GHz bandwidth and stores the resulting data in the

form of calibration tables. The third component is the Frequency Agile Target-Array Controller (FATAC), which has two main functions. First, it generates the timing signals for simulating up to 16 targets on each of the two programmable position array feeds and a single target on each of the two fixed position array feeds. Secondly, it generates signals to control amplifier selection, attenuator, and phase shifter values and switch settings to route the RF to the desired antenna on the CTS array. In generating these control signals, FATAC uses the calibration data to compensate for component variations that are a function of frequency. The FATAC has an interface to the FASP by which it obtains the correct frequency information.

Frequency Agile Target-Array Controller:

FATAC is the focal point of the digital and timing data required to set up and control the CTS programmable array (PA) in real time (Fig. 13). Achieving this task requires that FATAC hardware process the calibration data to develop the necessary PA steering commands, attenuation settings, and return delay values, along with the timing signals needed to generate the simulated radar target echoes. However, this is a complicated task. The commands and settings to the PA depend on the simulated target's current angle, range, amplitude, and on the transmitted frequency of the pulse during its associated pulse repetition interval (PRI). Since the frequency is not known until the instance of pulse transmission, all possible frequency/table variations must be accessible and able to be processed within a 2 μ s timeframe based on the minimum target simulated range. This is accomplished only by preloading all of the frequency associated calibration tables into FATAC processor's integrated memory. This memory, along with the associated algorithms and combinational logic, is resident on commercial off-the-shelf field programmable gate array (FPGA)-based circuit boards. The timing and synchronization signals are also generated by an FPGA-based circuit board that was custom designed and built by NRL. FPGA technology allows rapid redesign, customization, and scalability.

Summary: The Frequency Agile Target-Array Controller is a significant upgrade to NRL's laboratory simulation capability. It directly enables the development and evaluation of effective electronic countermeasure technologies for use against frequency agile missile threats to the U.S. Navy and provides a significant capability for continuing future research.

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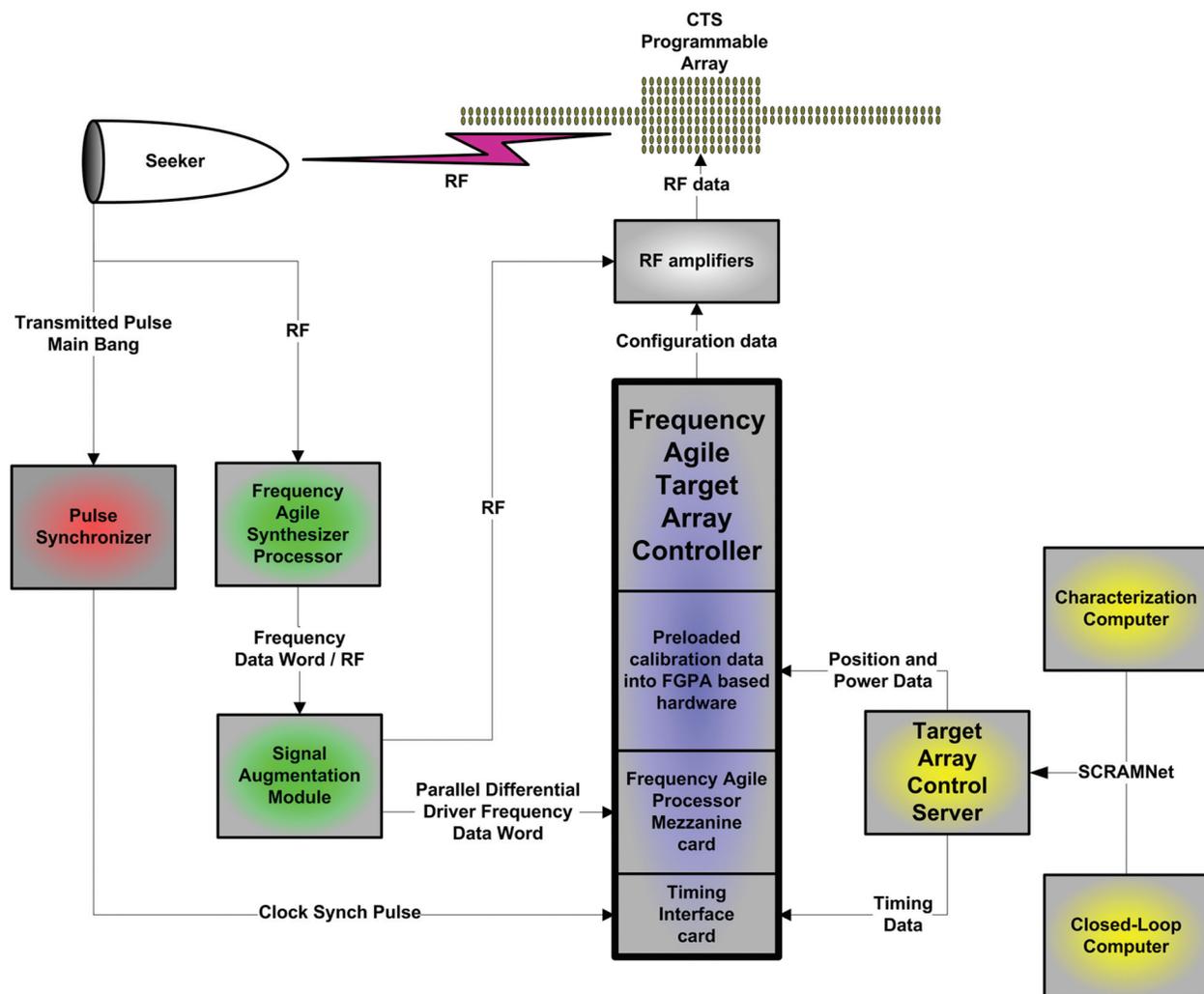


FIGURE 13
Data flow block diagram for a frequency agile simulation.