With Graphene Tunnel Barriers, Resistance Is Not Futile

Graphene, the two-dimensional, hexagonal lattice form of carbon discovered in 2004, has been revealing its unique properties ever since. It can be used as a highly effective atomically thin electrical conductor, but it also exhibits extraordinary out-of-plane resistance and spin transport. Although these properties have not been greatly studied, they might prove just as useful. NRL researchers are testing graphene's applicability as a tunnel barrier for transport perpendicular to the basal plane. With its out-of-plane resistance combined with its low spin-scattering, graphene is poised to become the material of choice in tomorrow's electronic technologies.

Graphene's excellent spin-transport quality is important in two ways: use of it should be able to provide a huge advancement in magnetic random access memory (MRAM) technology, and it should also revolutionize semiconductor spintronics. Today's MRAM devices' chips use magnesium oxide magnetic tunnel barriers on the chips; however, the use of graphene tunnel barriers instead on those chips should reduce resistance significantly, providing faster and smaller non-volatile memory. In semiconductor spintronics applications, graphene will enable a whole new field of electronically reconfigurable logic. Functions that are currently performed in dedicated hardware [Application-specific Integrated Circuits (ASICs)] could be taken over by software-driven reconfigurable logic. The low-resistance graphene provides the ability to change logic gates on a chip on the fly. The result will be more complex computing at a substantially lower power consumption. The potential savings in hardware and energy usage, along with the greatly increased flexibility of the resulting electronics, should provide not only astounding new commercial electronics but, more significantly, great advantage to the soldier in the field.

Graphene as a Tunnel Barrier

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Electrical transport in graphene, a single sheet of carbon atoms in a hexagonal lattice, has quickly become one of the most well-studied topics in materials science and condensed matter physics since initial reports of its discovery in 2004. The discovery stimulated a substantial redirection of international research effort in nanoscience, and ultimately led to the award of the Nobel Prize in physics in 2010.

While these efforts have focused on graphene's extraordinary in-plane charge carrier mobility and conductivity, the out-of-plane charge and spin transport of this remarkable material have not been addressed. Its parent compound, graphite, is known to have a strong conductance anisotropy — the weak interlayer coupling and wave function overlap produce relatively poor conductivity perpendicular to the basal plane. The combination of excellent lateral transport and low out-of-plane conductivity suggests that graphene could uniquely serve as both a low-loss medium for in-plane conduction as well as a tunnel barrier for transport perpendicular to the plane, providing a highly versatile single-material platform for future nanoscale devices. In addition, its low spin-orbit interaction results in low spin scattering, suggesting that graphene may be a key material for spin-based information storage and processing. Intriguingly, ferromagnet-graphene-ferromagnet structures have also been predicted to yield highly efficient spin-filtering properties due to band structure interactions and could find use in a variety of new spin-based technologies.

TECHNOLOGY BACKGROUND

The *International Technology Roadmap for Semiconductors* has identified the electron's spin angular momentum as a potential new state variable for semiconductor device operation for use beyond Moore's Law. Semiconductor spintronics aims to incorporate the electron spin in CMOS-like devices, such as the spin-MOSFET. New paradigms for spin-based devices, such as spin-FETs and reconfigurable logic, have been proposed and modeled. These devices rely on electron spin being injected, transported, manipulated, and detected in a semiconductor channel. These new spin-based technologies promise to combine the advantages of charge-based dynamic memory (speed, solid state) with those of magnetic storage (non-volatility, low power, radiation hardness). For example, spin-torque magnetic random access memory (ST-MRAM) based on magnetic tunnel junctions (MTJs) has made great advances in recent years through a better understanding of the science behind spin transport and manipulation, with the first commercial chips now available.

Future devices based on tunnel barriers will require much improved tunnel barrier materials. An ideal tunnel barrier should exhibit several key material characteristics: uniform, well-controlled thickness, minimal defect/trapped charge density, a low resistance-area product for minimal power consumption, and compatibility with adjacent materials, ensuring minimal diffusion to/from the surrounding materials at temperatures required for device processing. These requirements have remained beyond the reach of contemporary oxide-based tunnel barriers.

We show here that while graphene exhibits metallic conductivity in-plane, it serves effectively as an insulator for transport perpendicular to the plane, and provide the first demonstration of two potential applications. First we show how a single layer of graphene can be used as an atomically thin tunnel barrier in an MTJ, preserving the spin polarization of the electrons while providing thickness control unattainable with traditional oxide materials. We have measured out-of-plane transport through a single layer of graphene by fabricating metal-graphene-metal junctions using two ferromagnetic (FM) metals, in an MTJ structure.[1] We observe spin-polarized electron tunneling clearly measureable even above room temperature. Secondly, we demonstrate the use of graphene as a tunnel barrier for spin injection into a silicon channel. The spin-injection contact resistances achieved are three orders of magnitude lower than for comparable oxide tunnel barrier contacts and fall within a critical window of values required for practical devices.[2] These results enable realization of semiconductor spintronic devices such as spin-based transistors, logic, and memory.

GRAPHENE-BASED MAGNETIC TUNNEL JUNCTIONS

Fabrication: Standard micofabrication techniques are used to produce an array of NiFe bottom electrodes on a heavily oxidized silicon wafer. A single sheet of graphene grown by chemical vapor deposition (CVD) is transferred from its original copper foil substrate to the electrode array and patterned using deep-UV photolithography. The graphene's conductive edge states are buried in a layer of SiO_2 and a Co top electrode is deposited (see Fig. 1). This wafer-scale fabrication process was performed at NRL's Nanoscience Institute.

Results: Initial I-V characterization shows a non-Ohmic junction with the increased low-bias resistivity typical of tunnel junctions. The weak temperature dependence of the low-bias resistivity was used to confirm that transport occurs by tunneling. In canonical tunnel junctions, the resistance depends on the ability of electrons from the emitter to tunnel into available states of matching polarization in the collector (see Fig. 2). When the electrodes are oppositely magnetized, the majority-spin density of states in the emitter corresponds to the smaller minority-spin density of states in the collector and vice versa. Consequently, resistance is higher in the antiparallel configuration than in the parallel case, where majority-spin states in the electrodes have the same polarization. As NiFe and Co have different magnetic coercivities, we can align the electrodes parallel or antiparallel by varying an external magnetic field. The relation between junction resistance (tunneling magnetoresistance or TMR) and applied field (Fig. 3) shows the characteristic parallel/antiparallel/parallel switching behavior of an MTJ. At low temperatures and low drive biases, where the physics of tunneling is simplest and most evident, the TMR reaches two percent.

As the bias and temperature increase, the effect is reduced (see Fig. 4). Higher voltages impart electrons with more energy, enabling them to access more empty states in the collector electrode even in the antiparallel case, lowering the resistance. The exact behavior depends on the density of states of the collector electrode, and, thus, on which metal is the collector, producing an asymmetry in the forward vs reverse-bias dependence. Higher temperatures lower the spin-polarization of the metal surfaces through various mechanisms, similarly reducing the observed effect. We compare these measurements with an established model of temperature-dependent spin tunneling and observe good agreement using accepted parameters for the metals used.

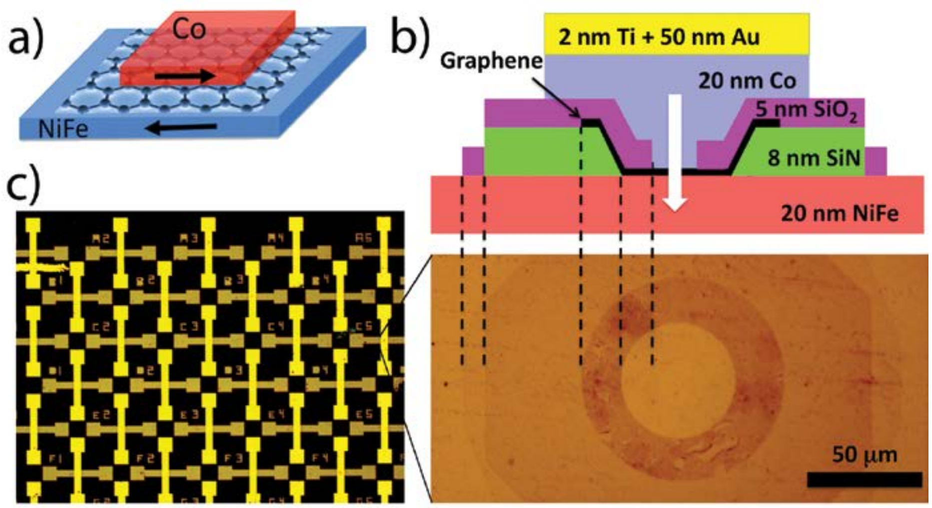

FIGURE 1
Depiction of graphene magnetic tunnel junctions. A conceptual schematic (a), cross-sectional diagram and corresponding top-view micrograph (without top metal), (b) and an optical micrograph of a completed structure (c).

GRAPHENE IN SEMICONDUCTOR SPINTRONIC DEVICES

In semiconductor spintronic devices, spin-polarized electrons are injected into a semiconductor channel, where the spins are transported, manipulated, and finally detected at the collector. Silicon (Si) is an attractive host for such a spin-based technology because of its technological importance as the backbone of modern electronics and because its low atomic mass and crystal inversion symmetry result in very small spin orbit interactions and long spin lifetimes.

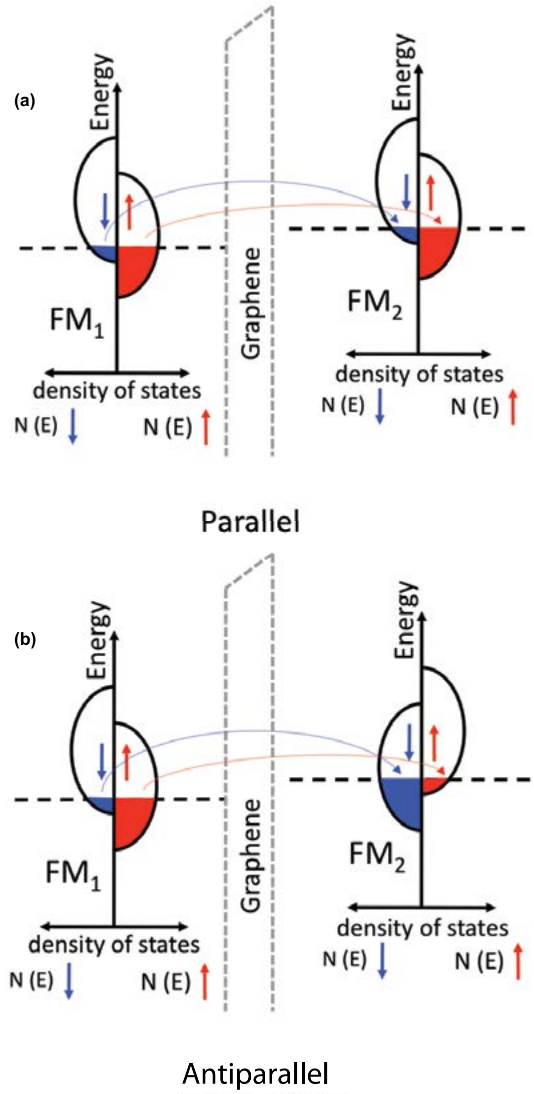

FIGURE 2
Magnetic tunnel barrier conceptual diagram, parallel vs antiparallel.

Ferromagnetic (FM) metals seem like the ideal candidates as contacts for electrical injection and detection of spin currents in the semiconductor channel. Any current in a ferromagnet is naturally spin-polarized at temperatures far above room temperature. However, keeping this spin polarization while the current is transferred from the ferromagnet into silicon is impossible due to the large difference in conductivity. A tunnel barrier between the FM metal and semiconductor was identified as a potential solution and extensive effort has been directed towards developing appropriate tunnel barriers for spin contacts. Most work has focused on either a reverse-biased FM Schottky barrier or an insulating oxide layer such as Al_2O_3 or MgO with a FM metal contact.

Metal Schottky barriers and oxide layers are susceptible to interdiffusion, interface defects, and trapped charge, which have been shown to compromise spin injection/transport/detection. FM metals readily form silicides even at room temperature, and diffusion of the FM species into the Si creates magnetic scattering sites, limiting spin diffusion lengths and spin lifetimes in the Si. Oxide barriers of atomic thickness contain unavoidable pinhole leaks. The additional thickness needed to avoid pinholes results in contacts with high resistance, increased power consumption, and contact resistances outside the window of resistance-area (*RA*) products essential for efficient spin injection/detection.

Graphene offers a compelling alternative — a single monolayer provides a much lower *RA* product than a film of any oxide thick enough to prevent pinholes (~ 1 nm). An FM metal/monolayer graphene contact can serve as a spin-polarized tunnel barrier contact that successfully circumvents the classic metal/semiconductor

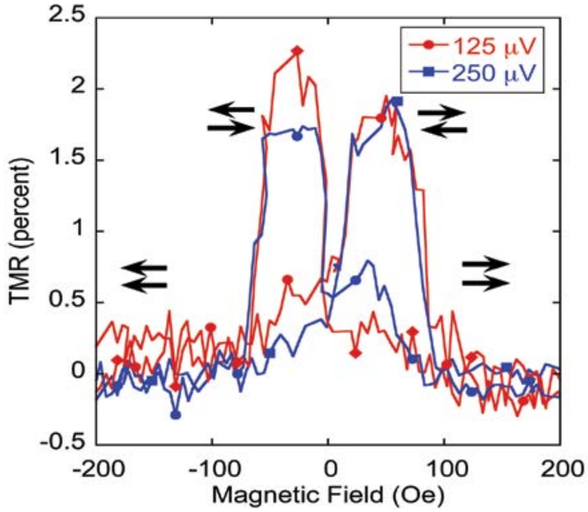

FIGURE 3
TMR of 2% at 0.25 mV.

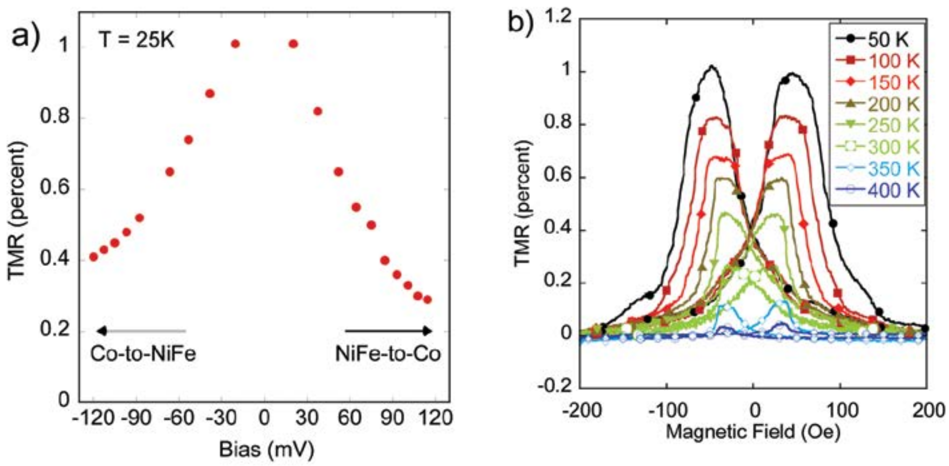

FIGURE 4
(a) TMR(V), (b) TMR(B) at various temperatures.

conductivity mismatch issue for electrical spin injection.

The Devices: Three types of tunnel barriers –SiO_2, Al_2O_3, and graphene — were fabricated on identical Si substrates. Here, 2 nm of SiO_2 was grown on HF etched Si using plasma oxidation to obtain pinhole-free barriers. Al_2O_3 tunnel barriers are routinely used in research grade and commercially available magnetic tunnel junctions. Here, a 1.5-nm-thick Al_2O_3 layer is grown in situ by a two-step natural oxidation process. Finally, graphene was grown by low-pressure CVD within Cu foil "enclosures" and transferred onto hydrogen-passivated n-type silicon. For this study, Si wafers with donor concentrations of 1×10^{19}, 3×10^{19}, and 6×10^{19} were used. The top electrode for all three types of tunnel barriers is sputter-deposited $Ni_{80}Fe_{20}$. Figure 5 is a schematic of the device used in this study.

The Results: Spin lifetime and spin diffusion lengths are important figures of merit for spin devices. For a practical device, the spin diffusion length ($L_{SD} = (D\tau_s)^{1/2}$) in the semiconductor channel has to be longer than the device dimensions. Hanle spin precession (caused by dephasing of electron spins in an applied magnetic field) measurements are used to determine spin lifetimes and spin diffusion lengths. The top three curves in Fig. 6 are the Hanle measurements of the Al_2O_3, SiO_2, and graphene tunnel barrier samples at room temperature. For all three barriers, a negative magnetoresistance was observed with a Lorentzian line shape caused by field-induced precession, confirming successful spin accumulation in silicon. The bottom two measurements of Fig. 6 are for the NiFe/Si(1×10^{19}) reference sample and a nonmagnetic/graphene/Si(1×10^{19}) control sample, measured at 10K. No magnetic field dependence is observed and none is

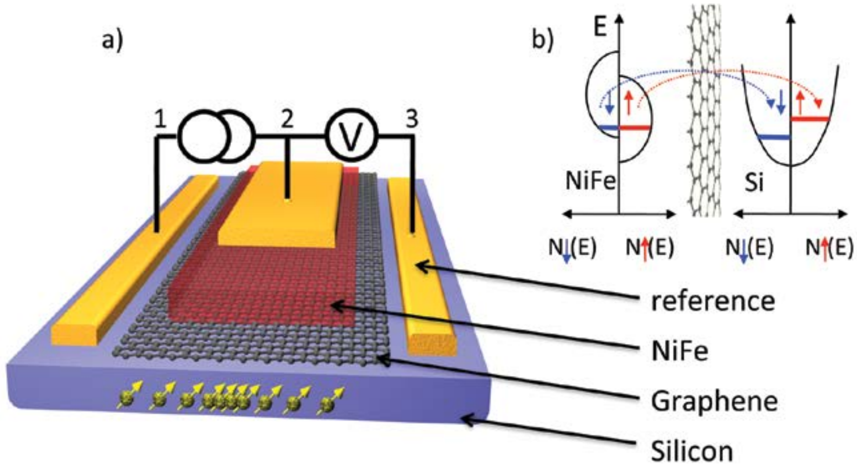

FIGURE 5
Schematic of the samples. (a) Monolayer graphene serves as a tunnel barrier between the FM metal contact and the Si substrate. Contacts 1 and 3 are Ohmic Ti/Au contacts. (b) Schematic illustrating spin injection and spin accumulation.

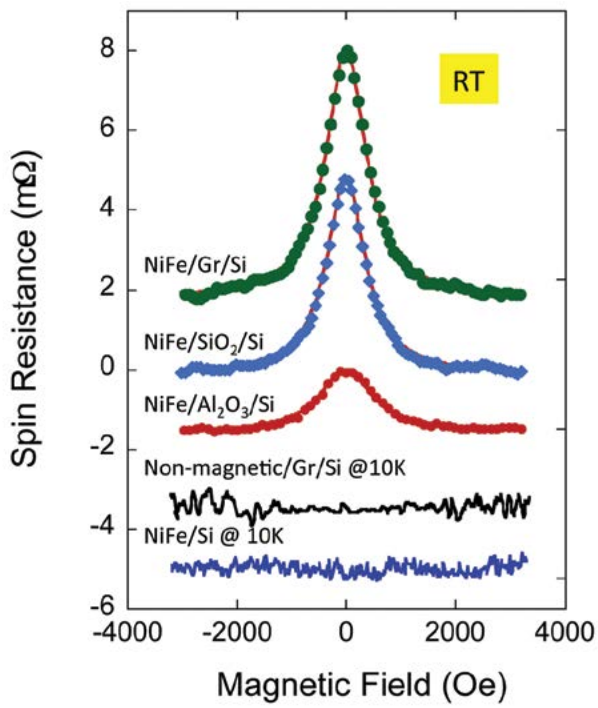

FIGURE 6
Hanle spin precession measurements; graphs are offset for clarity. Room temperature Hanle data for spin injection NiFe/Al_2O_3/Si (3×10^{19}) (red), NiFe/SiO_2/Si (3×10^{19}) (blue) and NiFe/Graphene/Si (1×10^{19}) (green). Also shown are the control samples; nonmagnetic/graphene/Si (1×10^{19}) and NiFe/Si (1×10^{19}) measured at 10 K.

expected. Although NiFe/Si(1×10^{19}) forms a Schottky contact and spin-polarized electrons could, in principle, tunnel across this barrier, silicide formation and diffusion of metallic ions from the NiFe are likely, suppressing spin injection for this contact. The top three Hanle curves can be fit with a Lorentzian lineshape given by $\Delta V_{3T}(B_z) = \Delta V_{3T}(0)/[1 + (\omega_L \tau_s)^2]$, where ω_L is the Lamor frequency and τ_s is the spin lifetime. Fits to this lineshape (shown in Fig. 6) give a lower bound of $\tau_s \sim 150$ ps for each of the tunnel barrier materials used (graphene, SiO_2, and Al_2O_3), demonstrating that the lifetime measured is not dominated by some characteristic of the tunnel barrier. This is also explicitly demonstrated in Fig. 7, where we plot the spin lifetime

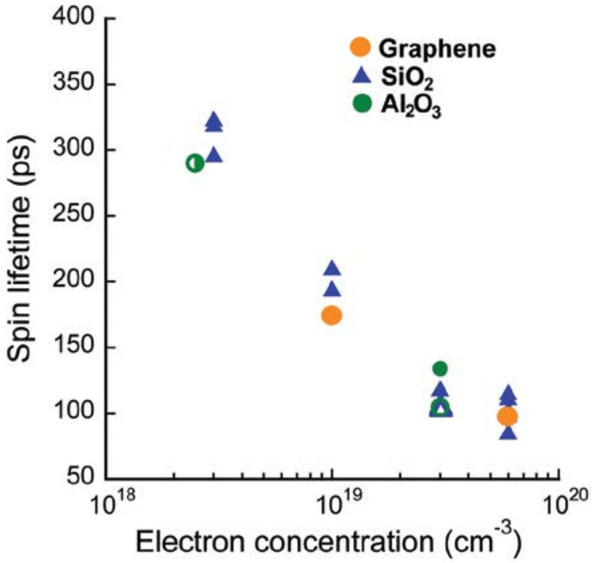

FIGURE 7
Spin lifetimes obtained from three-terminal Hanle measurements at 10 K as a function of the Si electron density for the tunnel barrier materials indicated and different ferromagnetic metal contacts (Fe, CoFe, NiFe). The symbol shape distinguishes the tunnel barrier material: triangles – SiO_2, green circles – Al_2O_3, and orange circles – graphene. Solid symbols correspond to devices with Ni0.8Fe0.2 contacts, half-solid symbols to Fe contacts, and open symbols to Co0.9Fe0.1 contacts. The spin lifetimes show a pronounced dependence on the Si doping level, and little dependence on the choice of tunnel barrier or magnetic metal.

obtained from three-terminal Hanle data on n-Si as a function of electron density for three different tunnel barrier materials (graphene, Al_2O_3, and SiO_2) and three different magnetic metal contacts (Fe, CoFe, and NiFe). The spin lifetime measured with the three-terminal Hanle geometry shows a clear dependence only on electron density, and the dependence is consistent with literature electron spin resonance data on bulk Si. The spin lifetime is completely independent of the tunnel barrier material or magnetic metal used for the contact. The values for the graphene tunnel barriers fall directly on the curve. These data confirm that the spin accumulation occurs in the Si, and not in the graphene or possible interface trap states.

The magnetic contact's conventional *RA* product is an important parameter in determining the practical application of a spin-based semiconductor device. Calculations have shown that significant local MR can be achieved only if the contact *RA* product falls within a range, which depends upon the Si channel conductivity, the spin lifetime, and the contact spacing. The *RA* products of all tunnel barrier contacts to date have been much larger than required, making such devices unattainable. However, the low *RA* products provided by the graphene tunnel barriers fall within this window, and enable realization of these and other important spintronic devices. We calculate the range of optimum *RA* products and the corresponding local MR as a function of the Si electron density using the contact geometry shown as the inset to Fig. 8. The geometric parameters are chosen to be consistent with the node anticipated for Si device technology within the next 5 years. The color code in Fig. 8 identifies the range of useful MR and the corresponding window of contact RA products required.

Tunnel barrier contacts of FM/AlOx and FM/SiO_2 fabricated in our lab on identical substrates have been shown to produce significant spin accumulation in Si, but have *RA* products that are too high to generate usable local MR. In contrast, using monolayer graphene as the tunnel barrier lowers the *RA* product by orders of magnitude, and values for the NiFe/graphene contacts on bulk wafers fall well within the range required to generate high local MR. Reducing the *RA* product

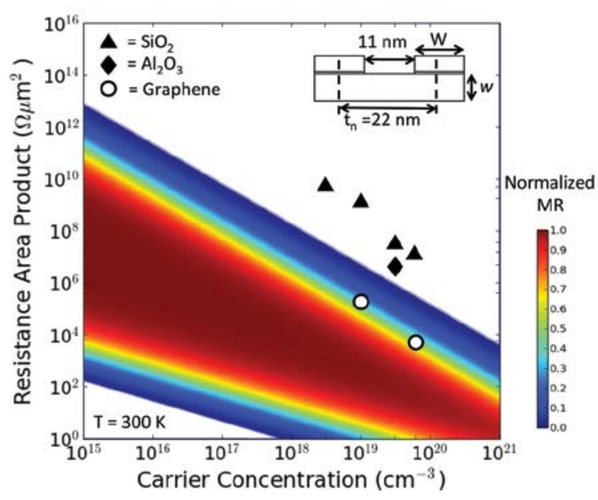

FIGURE 8
Calculation of the local (two terminal) magnetoresistance as a function of the contact's conventional *RA* product and the Si electron density for the device geometry shown in the inset. The data points are the *RA* products measured for our FM metal/tunnel barrier/Si contacts using 2-nm SiO_2 (triangles), 1.5-nm AlOx (squares), and monolayer graphene (circles) tunnel barriers prepared from identical Si wafers in our lab. The FM metal/graphene *RA* products fall within the window of useful MR values. In this figure, W and w both equal 11 nm.

also has a positive effect on the electrical properties of the spin device, as lowering the resistance reduces noise and increases the speed of an electrical circuit.

SUMMARY

This work is the first demonstration of the use of a single layer of graphene as a tunnel barrier. By incorporating a single layer of CVD-grown graphene into an MTJ structure, we've shown that charge and spin transport across the graphene occurs by tunneling and preserves the spin polarization of the tunneling carriers. Using FM-graphene tunnel contacts to inject spin into a silicon channel, we've shown that such contacts achieve dramatically lower resistance than equivalent oxide-based tunnel contacts. These discoveries pave the way for a new generation of spintronic devices using graphene in an unconventional way, but providing unparalleled potential for better than state-of-the-art performance.

ACKNOWLEDGMENTS

This work was supported by core programs at NRL, and the Office of Naval Research. EC and ALF gratefully acknowledge support through the NRL Karles Fellow program. The authors gratefully acknowledge the use of facilities in the NRL Nanoscience Institute, and thank David Zapotok and Dean St. Amand for continual technical support.

[Sponsored by ONR]

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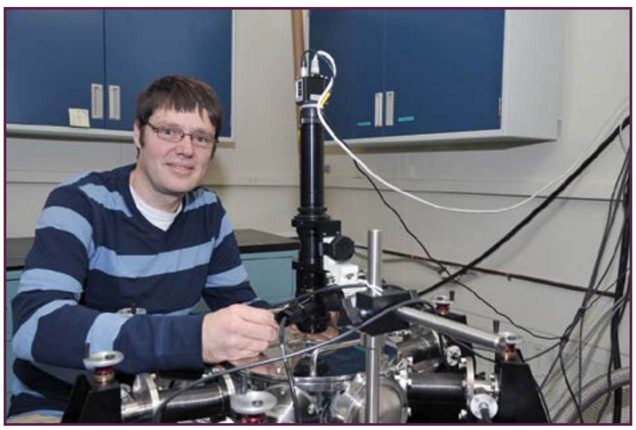

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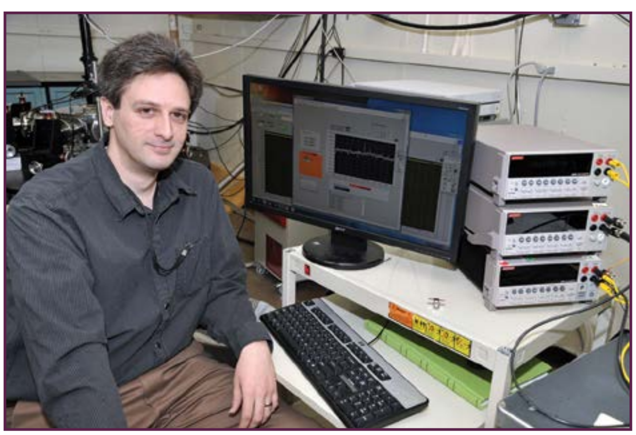

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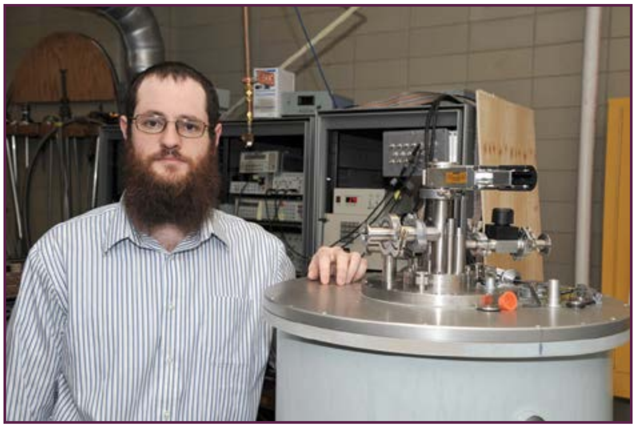

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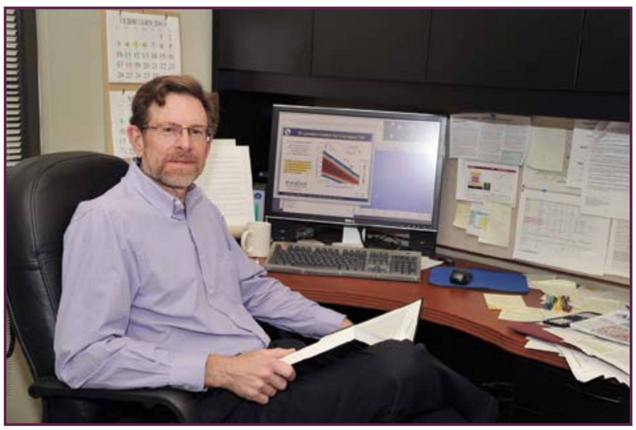

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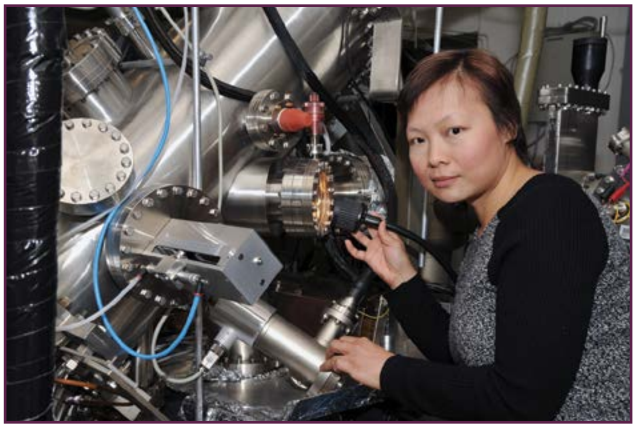
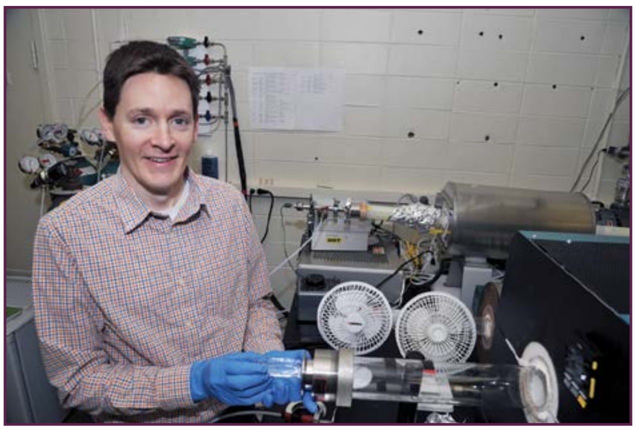


CONNIE H. LI received her B.S. and Ph.D. in 1998 and 2002, respectively, from the University of California, Los Angeles (UCLA), working on compound semiconductor surface reactions at an atomic scale in metal organic vapor phase epitaxy (MOVPE), during which she was supported by a National Science Foundation (NSF) Graduate Fellowship. She joined NRL as a National Research Council (NRC) Postdoctoral Research Associate in 2002 and became a staff research scientist in 2004 in the Magnetoelectronic Materials and Devices section in the Materials Science and Technology Division. Her current research involves spin-dependent transport and magneto-optical studies in magnetic semiconductors and ferromagnet/semiconductor heterostructures for spintronic applications. She has published 52 scientific papers and has given 15 invited talks. She has received three Alan Berman Research Publication Awards and an NRL Review Award.



JEREMY T. ROBINSON earned his bachelor's degree in physics from Towson University in 2002 and went on to study materials science and engineering at UC Berkeley. His Ph.D. research was centered on the direct self-assembly of germanium nanostructures on silicon surfaces. Upon finishing his Ph.D. in 2007, he worked for one year as an NRC postdoctoral fellow in the Electronics Science and Technology Division at the Naval Research Laboratory. Since joining the full-time staff in ESTD in 2008, his research activities have focused on the development of graphene-based materials and studying graphene's electronic, mechanical, and chemical properties.