A W-Band InAs/AlSb Low-Noise/Low-Power Amplifier

William R. Deal, *Member, IEEE*, Roger Tsai, Michael D. Lange, J. Brad Boos, *Member, IEEE*, Brian R. Bennett, and
Augusto Gutierrez, *Senior Member, IEEE*

Abstract—The first W-Band antimonide based compound semiconductor low-noise amplifier has been demonstrated. The compact 1.4-mm^2 three-stage co-planar waveguide amplifier with 0.1-μm InAs/AlSb high electron mobility transistor devices is fabricated on a 100-μm GaAs substrate. Minimum noise-figure of 5.4 dB with an associated gain of 11.1 dB is demonstrated at a total chip dissipation of 1.8 mW at 94 GHz. Biased for higher gain, 16 ± 1 dB is measured over a 77–103 GHz frequency band.

Index Terms—Antimonide-based compound semiconductor (ABCS), grounded coplanar waveguide (GCPW), low noise amplifier (LNA), millimeter-wave imaging.

I. INTRODUCTION

THE performance of low noise amplifiers (LNAs) is a critical aspect in microwave and mm-wave system designs. In addition to noise figure and gain, low dc power consumption is critical for large-scale array applications. The low-power low-noise characteristics of antimonide-based compound semiconductor (ABCS) high electron mobility transistor (HEMT) devices have the potential to supplant existing technologies with equivalent RF performance being achieved at $\sim 10\%$ of the dc power compared to GaAs and $\sim 25\%$ compared to InP [1].

The system designs of satellite radar systems, such as the space based radar (SBR) in [2], are particularly power constrained. With element numbers of 10^5 to 10^6 elements, reduction in LNA dc power from 10 mW to 1 mW would result in a dc power reduction on the order of kW per system, with dramatic implications on the size, weight, and cost of such systems.

ABCS HEMT devices also demonstrate excellent mm-wave performance. At mm-wave frequencies, passive millimeter-wave focal plane cameras such as the 1040-element densely packaged system reported in [3] require an active liquid cooling system to manage thermal dissipation. The eight stage receiver monolithic microwave integrated circuit (MMIC) consumes 160-mW per focal plane element [4], or 20-mW per GaAs MMIC stage. The ABCS MMIC amplifier reported in this letter consumes only 0.6 mW per stage at optimal noise bias, only 3% of the per stage power consumption of the GaAs
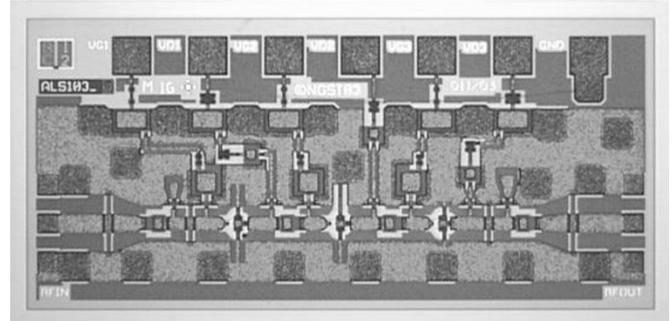
Fig. 1. Microphotograph of W-band three-stage GCPW ABCS HEMT low-noise amplifier. Die size is 1700×800 μm.

MMIC operating at the same frequency band. The front-end of a comparable ABCS-based imaging array could therefore use less than 5 W, compared to the 160-W used by the existing GaAs-based array front-end in [2]. Additionally, since this is a passive system, the lower linearity from operating at a lower dc operating point should have little impact. A microphotograph of the ABCS MMIC LNA is shown in Fig. 1.

Development of InAs-channel devices is challenging due to the lack of viable semi-insulating substrates for lattice-matched growth. Metamorphic growth using the $Al_X Ga_{1-X} Sb_Y As_{1-Y}/InAs$ material system, with a lattice constant near 6.1 Å, has proven to be a viable alternative for state-of-the-art InAs-channel HEMTs [5], [6] and researchers in this field now routinely achieve electron mobility $> 20\,000$ cm^2/V-s with tensile strained InAs channels. However, the approach does hold several unique challenges such as intrinsic material stability, gate leakage, and yield limiting defect densities, which have been incrementally addressed over the years [7]. Recently, the first AlSb/InAs MHEMT based MMICs have been demonstrated, including a single-stage X-band amplifier [8] and a three stage Ka-Band LNA [9].

II. ABCS HEMT DEVICES

The AlSb/InAs MMICs were grown by molecular beam epitaxy on low-cost semi-insulating 3-in GaAs substrates. Our standard profile with optimization of the MBE flux conditions and modulation doping has achieved an average sheet resistance of 200.9 Ω/sq with less than 2.6% nonuniformity and 300 K mobility of $26\,300$ cm^2/V * s with electron sheet density of 1.28×10^{12} cm^{-2} [1].

DC tests of devices have shown high transconductance at low drain-source voltages. The average G_m peak was 1.05 S/mm and 2.56 S/mm measured at a V_{DS} of 0.2 V and 0.4 V, respectively.
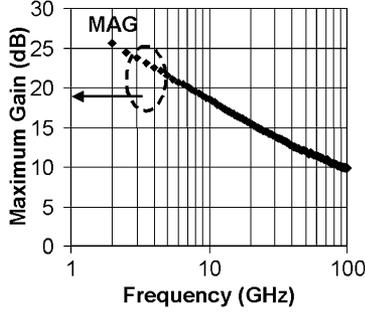
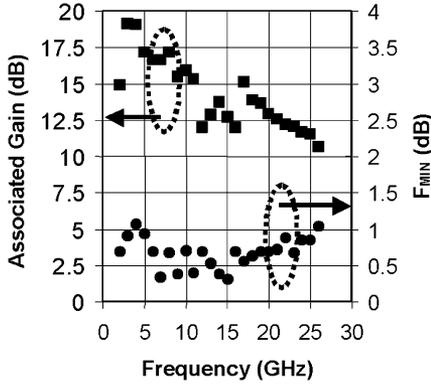Fig. 2. Maximum available gain for two-finger device with 40-μm periphery.

Fig. 3. Measured 2–26 GHz associated gain (G_A) and minimum noise figure (F_{MIN}) at $V_{\mathrm{DS}} = 0.2$ V and 6-mW/mm dc dissipation.

Small signal RF tests have shown maximum available gains greater than 10 dB at 100 GHz and $f_{\max}$ higher than 270 GHz measured at V_{DS} of 0.4 V and 112-mA/mm for a two-finger, 40-μm device. Maximum available gain is shown in Fig. 2. We have also measured average peak f_T of 153 GHz and 212 GHz at V_{DS} of 0.2 V and 0.4 V and drain current densities of 114 and 340 mA/mm, respectively. Noise performance of the device, shown in Fig. 3 up to 26 GHz, shows a minimum noise figure of 0.85 dB and associated gain of 11.5 dB at an ultra-low bias point of V_{DS} at 0.2 V and 6 mW/mm. These RF characteristics are sufficient for performance into the millimeter-wave region.

III. AMPLIFIER DESIGN

The three-stage amplifier is designed using two finger devices with a periphery of 40-μm per device. For low noise design, a small signal model with noise contribution is used. The model was developed using S-parameters and noise parameter measurements to 50-GHz, with performance at W-band extrapolated from the fitted model.

The amplifier is designed using grounded coplanar waveguide (GCPW) transmission lines and passive components for operation on a 100-μm GaAs substrate. Parameterized models for GCPW structures and discontinuities including MIM and TFR are developed from EM simulations. No EM simulations are used explicitly in the design.

The broadband amplifier is optimized to cover the majority of W-Band with simulated gain of $\sim 12 \pm 0.5$ dB from 80–110 GHz when biased at a device V_{DS} of 0.2 V and drain current of 1.2 mA/stage. A C-R-C (0.2 pF-35 Ω-1 pF) network in the drain biasing networks is used to reduce the low
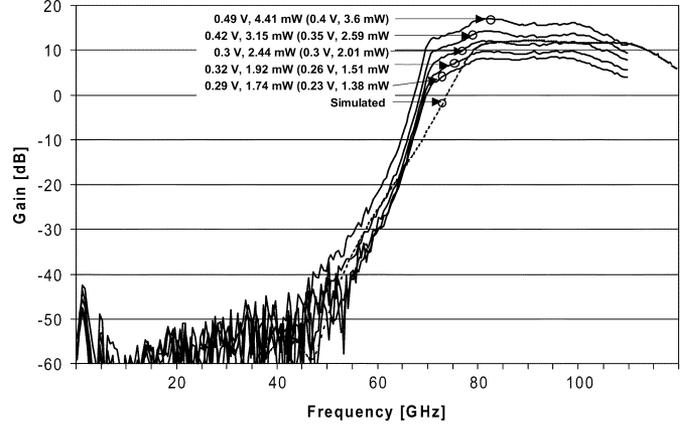

Fig. 4. Measured and modeled gain across bias. Pad voltage and power are indicated at each bias point. Device Vds and power indicated in parenthesis.

frequency gain with minimal impact at the high end of the amplifier band. The 0.2-pF GCPW capacitor provides sufficiently low impedance to ground at 110 GHz for low loss bypassing, but is a poor enough bypass at lower frequencies (50–70 GHz) so that the gain is attenuated by the 35-Ω resistor and second 1-pF bypass, yielding a flat gain response without sacrificing high-end gain and noise figure. A comparatively larger bypass capacitor (0.75 pF) is used in the gate bias network to minimize noise figure degradation. An open-circuited GCPW stub is used at both the input and output to further improve matching. Inductive lines at the source of the transistors in the first and second stage are used to bring Γ_{opt} closer to 50 Ω. Very little inductance is used at the third stage to maximize the gain of that stage. Also visible in Fig. 1 are parallel rows of vias used for suppression of undesired substrate modes that can reduce gain. In this circuit, a fairly regular via spacing of $\lambda/8$ in the substrate is used. Although there is some risk of a resonance occurring when a periodic via spacing is used, out of band gain reduction is good enough that this should not be a problem.

IV. MEASURED RESULTS

After processing, the W-Band ABCS MMIC LNA has been measured using an on-wafer probe station. First, performance over bias is measured. All drain bias pads are held to the same voltages and each individual gate voltage is adjusted so that each stage draws identical drain current. S-Parameters were taken from 0.5–110 GHz. Measured and modeled gain are shown in Fig. 4. at various bias points. There is a modest downward shift in frequency of the gain response. For a first pass W-Band design using device models extracted from measurements below 50 GHz, this shift is judged to be moderate. Error is likely due to either device modeling error, passive circuit modeling error or processing variation. Note that the bias conditions for each measured trace are indicated in the figure, with drain voltage and power dissipation de-embedded to the device indicated in parenthesis. Note that the highest measured gain is 16$\pm$ 1-dB from 77 to 103 GHz. The biasing condition for this gain is a pad voltage of 0.49 V and a total MMIC dissipation of 4.41 mW. The V_{DS} is back calculated to be 0.4 V and a total device dissipation of 3.6 mW for all three stages. Measured and modeled input
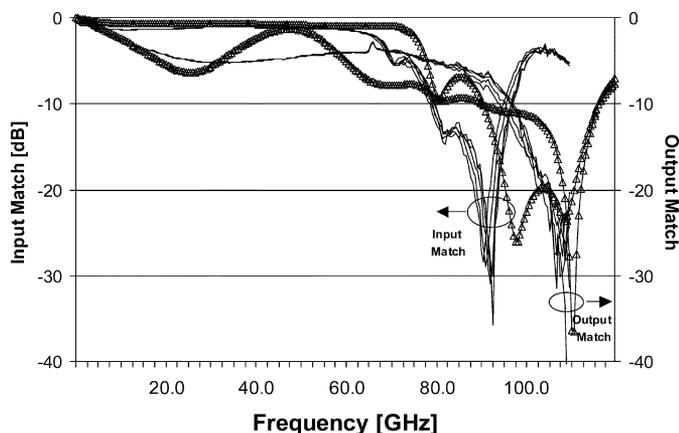
Fig. 5.   Measured and modeled input and output match at various bias points. Triangular markers indicate simulated responses.
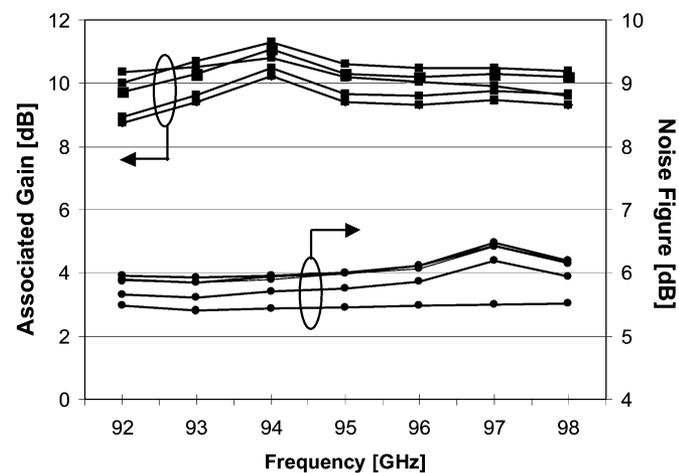

Fig. 6.   Measured noise figure and associated gain for chip biased at a pad voltage of 0.3 V and drain current of 2 mA/stage.

and output match are shown in Fig. 5 for the same biasing conditions. Again, agreement is good with the input match showing a shift downwards of approximately 10%.

Noise figure and associated gain are measured on wafer for several sites as shown in Fig. 6. The minimum noise-figure for the MMIC is obtained at a drain pad voltage of 0.3 V ($V_{DS}=$ 0.225 V) and a drain current of 2-mA/stage, corresponding to a total chip dissipation of 1.8 mW with 1.35 mW dissipated by the devices. Under these bias conditions, minimum noise figure of 5.4 dB is measured at 94 GHz with an associated gain of 11.1 dB. Note that no effort was made to independently optimize

the bias of each stage, which we anticipate should yield modest additional improvement.

V. CONCLUSION

In this letter, the first reported W-Band LNA using ABCS HEMTs is reported, and achieves a respectable 5.4-dB noise figure at 94 GHz with an associated gain of 11.1 dB at an ultra-low dc power of 1.8 mW. When biased for higher gain, it achieves 26 ± 1-dB gain over a 25-GHz bandwidth at a total chip dissipation of 4.41 mW. This validates the ABCS technology as a viable candidate for ultra-low power, low noise applications into the millimeter-wave regime.

ACKNOWLEDGMENT

REFERENCES

[1] R. Tsai, R. Grundbacher, M. Lange, J. B. Boos, B. R. Bennett, P. Nam, L. J. Lee, M. Barsky, C. Namba, K. Padmanabhan, S. Sarkozy, P. H. Liu, and A. Gutierrez, "Manufacturable AlSb/InAs HEMT technology for ultra-low power millimeter-wave integrated circuits," in *Proc. Mantech Conf.*, 2004, pp. 69–72.
[2] S. Fiedler and B. Preiss, "Geosynchronous space based radar concept development for theater surveillance," in *Proc. IEEE Aerospace Applications Conf.*, vol. 4, Feb. 1996, pp. 77–90.
[3] G. S. Dow, D. C. W. Lo, Y. Guo, E. W. Lin, T. T. Chung, M. D. Biedenbender, O. Miromontes, A. Marashi, L. Yujiri, P. S. C. Lee, M. M. Soucri, and B. R. Allen, "Large scale W-band focal plane array for passive radiometric imaging," in *IEEE MTT-S Dig.*, 1996, pp. 369–373.
[4] G. S. Dow, T. N. Ton, H. Wang, D. C. W. Lo, W. Lam, B. Allen, K. Tan, and J. Berenz, "W-Band MMIC direct detection receiver for passive imaging systems," in *IEEE MTT-S Dig.*, 1993, pp. 163–166.
[5] J. B. Boos, W. Kruppa, B. R. Bennett, D. Park, S. W. Kirchoefer, R. Bass, and H. B. Dietrich, "AlSb/InAs HEMTs for low-voltage high-speed applications," *IEEE Trans. Electron Devices*, vol. 45, no. 9, pp. 1869–1875, Sep. 1998.
[6] K. Yoh, T. Moriuchi, and M. Inque, "An InAs channel heterojunction field-effect transistor with high transconductance," *IEEE Electron Device Lett.*, vol. 11, no. 11, pp. 526–528, Nov. 1990.
[7] C. R. Bolognesi, "Antimonide-based high-speed electronics: A transistor perspective," in *Proc. Indium Phosphide Related Materials Conf.*, 2002, pp. 55–58.
[8] R. Tsai, M. Barsky, J. B. Boos, B. R. Bennett, J. Lee, N. A. Papanicolaou, R. Magno, C. Namba, P. H. Liu, D. Park, R. Grundbacher, and A. Gutierrez, "Metamorphic AlSb/InAs HEMT for low-power, high-speed electronics," in *Gallium Arsenide Integrated Circuit Symp. Technical Dig.*, 2003, pp. 294–277.
[9] J. B. Hacker, J. Bergman, G. Nagby, G. Sullivan, C. Kadow, H. K. Lin, A. C. Gossard, M. Rodwell, and B. Brar, "An ultra-low power InAs/AlSb HEMT Ka-band low-noise amplifier," *IEEE Microw. Wireless Compon. Lett.*, vol. 14, no. 4, pp. 156–158, Apr. 2004.