Enhancement-mode metal-oxide-semiconductor single-electron transistor on pure silicon

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The authors demonstrate a silicon-based single-electron transistor (SET) in the few-electron regime. Our structure is similar to a metal-oxide-semiconductor field-effect transistor. The substrate, however, is undoped and could be isotope enriched so that any nonuniformity and spin decoherence due to impurity and nuclear spins can be minimized. A bilayer-gated configuration provides flexibility in manipulating single electrons. The stability chart measured at 4.2 K shows diamondlike domains with a charging energy of 18 meV, indicating a quantum dot of 20 nm in diameter. The benefits of using this enhancement-mode SET in silicon and its potential application for scalable quantum computing are discussed. © *2006 American Institute of Physics*.
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A number of physical implementations for qubits have been proposed and investigated as the bases for quantum computing.[1] Solid state implementations have potential for scaling, an important criterion for practical applications, and therefore they are attracting much attention. In particular, the two Zeeman states of an electron spin in a quantum dot (QD) offer a promising candidate[2] as a qubit, and lateral arrays of quantum dots provide an opportunity for scaling up to large numbers of qubits and quantum gates. A single electron confined in ^{28}Si QDs is expected to have a spin coherence time many orders of magnitude longer than that in, e.g., GaAs, due to the zero nuclear spin in ^{28}Si.[3] In addition, lateral quantum dots in silicon have the advantage of being easily incorporated into existing large-scale integrated circuits. In contrast to placing donors in silicon,[4] quantum dots promise controllable physical parameters. Nonetheless, there remain considerable challenges in fabricating quantum dots in silicon.

Since the first observation of Coulomb blockade tunneling in silicon,[5] experimental efforts have focused on depletion-mode field-effect transistor (FET) scheme, which use silicon-on-insulator[6] (SOI) wafers and Si/SiGe quantum well structures.[7–9] In these approaches, the sample contains a two-dimensional (2D) electron gas from donors in the system prior to nanofabrication. Surface Schottky gates or in-plane side gates are used to define QDs and to deplete electrons in QDs from many down to 1. Although this depletion-mode approach has been applied in GaAs single-electron transistors (SETs),[10] fabrication of silicon-based SETs still suffer from problems that arise from material deficiency. For example, gate leakage current due to dislocations in Si/SiGe quantum wells frequently disrupts the single electron transport. In the SOI approach, the defects at the silicon-buried oxide interface cause strong localization of electrons and result in a noisy environment.

In this letter, we report an experimental demonstration of metal-oxide-semiconductor SET (MOS-SET) using pure silicon substrates with two layers of metal gates. Our ultimate objective is to confine single electrons in an environment with a minimal concentration of impurities. In order to define precisely the location of a single spin and to consistently control the shape of the confinement potential by gating, the sample system should be free of random potential variations resulting from ionized impurities. An impurity-free environment will also reduce telegraph noise and spin decoherence via hyperfine interaction with impurity nuclear spins. To achieve this goal, high purity silicon wafers could be used. Because of the nonconducting initial state of our devices, we employ a bilayer-gated configuration to fabricate MOS-SETs. As illustrated in Figs. 1(a) and 1(b), the top gate, which laterally overlaps with the Ohmic contact regions, induces 2D electrons at the silicon-thermal oxide interface and the device behaves as an enhancement-mode FET.[11] In addition, multiple side gates, which are located below the top gate and above the thermal oxide, are used to deplete electrons below. Proper biasing of these gates defines the potential profile [as shown in Fig. 1(c)] of a SET, which inlcudes source and drain leads, two tunneling barriers, and a quantum dot in between. This bilayer design offers flexibility in device layout and allows independent control over the 2D electron density, the tunneling conductance, and the electron population in the quantum dot.

Applying our design concept, we have fabricated MOS-SETs that show no measurable gate leakage current (<10 fA) and display single electron tunneling phenomena. We used substrates that were p doped to approximately $10^{15}/\mathrm{cm}^3$ in a proof-of-principle demonstration. Higher resistivity wafers would further reduce impurity-induced disorder. We first defined Ohmic contact patterns by photolithography, followed by phosphorous ion implantation. The

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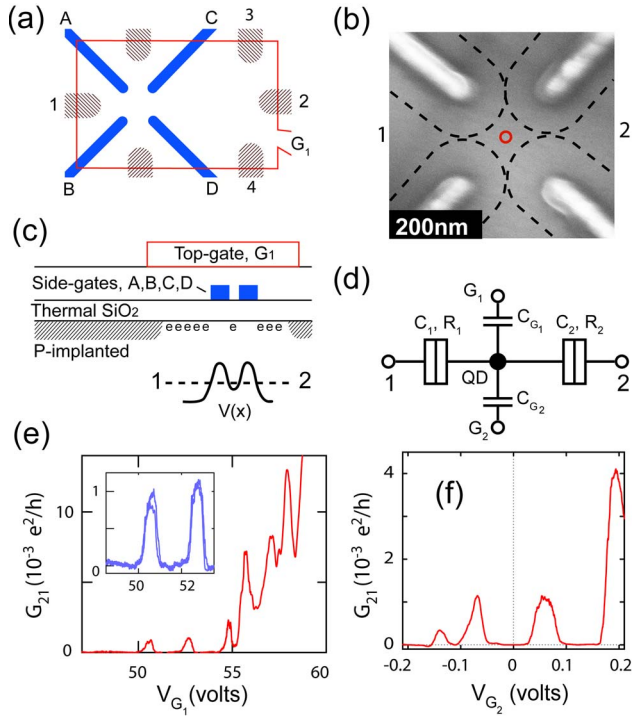

FIG. 1. (Color online) Schematics show (a) the top and (c) the cross sectional views of our silicon single-electron transistor structure. In (a) the solid thick line, the shaded regions, and the rectangular area depict the side gates, phosphorous-implanted Ohmic leads, and the boundary of the top gate, respectively. The schematic potential profile along the 1-2 direction under single electron tunneling condition is shown as the inset (lower right) in (c). (b) Scanning electron micrograph of 70-nm-wide side gates defined by electron-beam lithography, taken before the top gate is defined. The gap between neighboring side gates is ~160 nm. The dashed lines illustrate the depletion region under single-electron transistor operating condition. The 20 nm diameter circle depicts the location of the quantum dot as discussed in the text. (d) The SET equivalent circuit used in the analysis for capacitances. (e) Transfer characteristics vs the top-gate voltage at $V_A=V_B=V_C=V_D=0$ V and $V_{21}=8$ mV. The inset shows the up and down traces. (f) Transfer characteristics controlled by the side-gate voltage at $V_{G_1}=54.25$ V and $V_{21}=8$ mV.

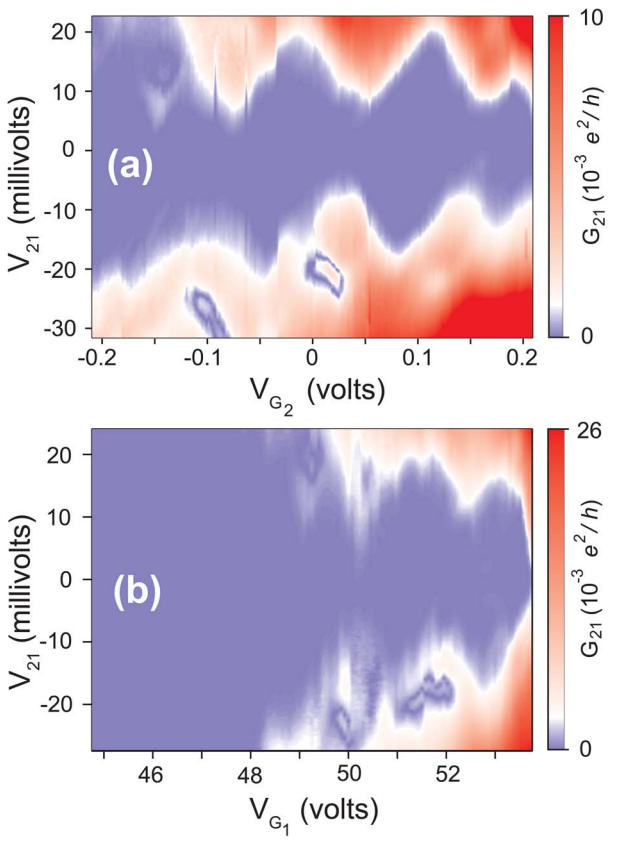

FIG. 2. (Color online) (a) The stability chart taken with $V_{G_1}=54.25$ V and with the side-gates swept between −32 and +22 mV. (b) The stability chart taken with all side gates shorted to zero and with V_{G_1} swept between 44.75 and 53.75 V.

Ohmic contact patterns are long leads extending from 3-μm-wide lines in the immediate SET device area to the 250 μm square bonding pads. A subsequent annealing for implant activation is carried out concurrently with the growth of thermal oxide. We choose to grow the thermal oxide at 1000 °C for 20 min in dry oxygen environment. This oxidation recipe results in a thermal oxide thickness of 27 nm and a sheet resistance of 63 Ω/□ in the patterned, implanted region. Then the SET side gates are defined by electron-beam lithography, followed by metal evaporation (aluminum and gold) and lift-off. Using a bilayer poly(methyl methacrylate) in the electron-beam lithography process, we are typically able to fabricate 70-nm-wide metal gates. Figure 1(b) shows the micrograph of one such example. Finally the top gate is defined by photolithography using negative tone resist on the top of the second layer of gate dielectric. We have tried different gate dielectrics, and the data presented here are from a device with 1-μm-thick spin-on polymer, Benzocyclobutene (BCB).[12]

These MOS-SETs are characterized at 4.2 K. While the source-drain, side gates, and the top gate are dc biased by digital-analog converters, the source-drain conductance is measured by an ac technique using a 37 Hz, 0.1–1 mV excitation voltage. The drain-source current is fed into a transimpedance amplifier with a gain of 100 MΩ followed by a lock-in amplifier. We first sweep the top-gate voltage (V_{G_1}) and monitor G_{34} [the conductance between Ohmic contacts 3 and 4 shown in Fig. 1(a)], and we find that the onset of strong inversion occurs at $V_{G_1}=44$ V. In contrast, we find that $G_{21}=0$ for $V_{G_1}<48$ V, which is due to the depletion region caused by the four side gates. Coulomb blockade oscillations dominate the G_{21} vs V_{G_1} characteristics for $50\ \text{V} \leqslant V_{G_1} \leqslant 55$ V. Figure 1(e) shows an example of Coulomb blockade oscillations where G_{21} versus the top-gate voltage is measured at $V_A=V_B=V_C=V_D=0$ V and $V_{21}=8$ mV (source-drain dc bias). The inset shows the reproducibility of the up and down traces, suggesting that the device is stable. Figure 1(f) presents another example in which the top-gate voltage is fixed and G_{21} is measured against the sweeping side-gate voltage.

We estimate that there are at most a few electrons under the measurement conditions used here. Based on the capacitive coupling between the top gate and the Si/SiO_2 interface, we calculated that the induced 2D electron concentration is 1.4×10^{10} V^{-1} cm^{-2}. The top-gate threshold voltage is 44 V, indicating that at $V_{G_1}=54.25$ V [the bias used in data shown in Fig. 2(a)] there is only one electron per 26×26 nm^2 area, which is on the same order as the size of the QD confinement. This estimate is also supported by the large charging energy as discussed below.

Figure 2(a) displays the stability chart of a SET, i.e., the contour plot of the drain-source conductance G_{21} versus the dc component of the drain-source bias (V_{21}) and side-gate

voltages ($V_{G_2}=V_A=V_B$, while $V_C=V_D=0$ V), with $V_{G_1}=54.25$ V. The unused Ohmic leads are left open. The contour plot shows a series of diamond-shaped blocks that is a manifestation of single electron transport in the Coulomb blockade regime. A similar stability chart, shown in Fig. 2(b), is obtained by fixing the side-gate voltages to 0 V (i.e., $V_A=V_B=V_C=V_D=0$ V), and sweeping the top-gate voltage (V_{G_1}). We model the SET by an equivalent circuit, shown in Fig. 1(d), which consists of a source (1), a drain (2), a QD, a top gate (G_1), and a side gate (G_2). There is capacitive coupling between the QD and the other electrodes, including the source (C_1), the drain (C_2), the top gate (C_{G_1}), and the side gates (C_{G_2}). To allow for tunneling conductance, two conductors connect the QD to the source (R_1) and the drain (R_2), accompanied by capacitors C_1 and C_2.

Applying the "orthodox" theory to the data shown in Fig. 2, the half height of the diamond ($\Delta V_{21}=e/C_\Sigma$) is a measure of the charging energy E_c ($=e^2/C_\Sigma$), where $C_\Sigma=C_1+C_2+C_{G_1}+C_{G_2}$. A charging energy of 18 meV is observed. The half height, the full width, and the two slopes defining the observed diamond also uniquely determine the respective capacitances: $C_1=4.3$ aF, $C_2=3.4$ aF, $C_{G_1}=0.08$ aF, and $C_{G_2}=1.3$ aF. If we model the quantum dot as a disk with a diameter d, the resulting capacitance of our silicon quantum dot suggests an effective diameter of about 20 nm. Here, we use $C_\Sigma=4\varepsilon d$ and $\varepsilon=11.9$ for the dielectric constant of silicon. A 20-nm-diameter circle is shown in Fig. 1(b). The QD that results from electrostatic confinement can be further downsized by using a thinner thermal oxide, narrower side gates, and smaller gaps between side gates. For qubit applications, a large energy level spacing is preferred because it decreases the mixing of orbital states by spin-orbit coupling, and consequently it reduces spin dephasing.[13] If we approximate the QD potential by a 2D harmonic oscillator, with a ground state wave function spread of 20 nm, the level spacing is ~7.8 meV. Compared to GaAs SETs, this energy spacing is large, despite a larger electron mass in silicon ($0.19m_0$ vs $0.067m_0$). Note that the spin-orbit coupling in silicon is three orders of magnitude smaller.[14] In other words, any spin dephasing mechanism via spin-orbit coupling[15] is three orders weaker in pure silicon, leading to a much longer spin lifetime.

In conclusion, we have demonstrated experimentally a silicon single-electron transistor with only a few electrons in the quantum dot. Our fabrication does not have the problems seen in other approaches,[6–9] such as gate leakage or severe disorder in the environment. The key features of this design include (1) the use of undoped substrates for removing impurity disorder and (2) MOSFET-like structures where electrons residing at the silicon-thermal oxide interface are induced and manipulated by two layers of gates. We demonstrate that the top gate and the nanofabricated side gates can be properly biased to create a single-electron transistor with a large charging energy. Because the two-layered gates control the single electron population and the tunneling barriers independently, this approach provides flexibility in regulating the number of electrons in the quantum dot. Future improvements could include using a lower background impurity concentration (e.g., $<10^{12}/\mathrm{cm}^3$) and a more refined thermal oxide growth technique to reduce further the electron traps in the system. Ultimately ^{28}Si enriched substrates could be used to minimize dephasing by nuclear spins. The top gate and the side gates can be nanoscaled so that the patterned electrons at the two-dimensional interface can form one-dimensional quantum wires or zero-dimensional quantum dots. This work suggests that using the bilayer-gating scheme on undoped silicon or on any quantum well heterosystems one can produce low dimensional electron systems of the highest quality.[15]

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