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# InAlSb/InAs/AlGaSb Quantum Well Heterostructures for High-Electron-Mobility Transistors

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Heterostructures for InAs-channel high-electron-mobility transistors (HEMTs) were investigated. Reactive AlSb buffer and barrier layers were replaced by more stable $Al_{0.7}Ga_{0.3}Sb$ and $In_{0.2}Al_{0.8}Sb$ alloys. The distance between the gate and the channel was reduced to 7–13 nm to allow good aspect ratios for very short gate lengths. In addition, $n^+$-InAs caps were successfully deposited on the $In_{0.2}Al_{0.8}Sb$ upper barrier allowing for low sheet resistance with relatively low sheet carrier density in the channel. These advances are expected to result in InAs-channel HEMTs with enhanced microwave performance and better reliability.

**Key words:** InAs, high-electron-mobility transistors (HEMTs), molecular beam epitaxy (MBE), FET, InAlSb, AlGaSb

## INTRODUCTION

High-electron-mobility transistors (HEMTs) with InAs channels and AlSb barriers were first reported over 15 years ago, as discussed in a recent review.[1] Advantages of this material system include the high electron mobility (30,000 $cm^2/V$ s at 300 K) and velocity ($4 \times 10^7$ cm/s) of InAs and a large conduction band offset between InAs and AlSb (1.35 eV). The large offset results in good carrier confinement and enhanced radiation tolerance.[2] There has been renewed interest in recent years. For example, two groups have achieved 100-nm-gate-length InAs-channel HEMTs with unity-current-gain cutoff frequency, $f_T$, and unity-power-gain cutoff frequency, $f_{max}$, values of 200–300 GHz.[3,4] Compared to state-of-the-art InP-based HEMTs with the same gate length, the InAs HEMTs provide equivalent high-speed performance at 5–10 times lower power dissipation.[4] These transistors exhibit low microwave noise, with noise figures of 0.6–0.8 dB at 10 GHz.[1] High-frequency performance has also been achieved in antimonide-free InAs-channel HEMTs with InAlAs barriers,[5,6] as well as InSb-channel HEMTs.[7] In the last 3 years, circuits based upon InAs HEMTs have been reported in the S-band,[8] X-band,[9,10] Ka-band,[11] and W-band.[5,12,13] For example, a three-stage W-band low-noise amplifier (LNA) was demonstrated with 11 dB gain at a total chip dissipation of only 1.8 mW at 94 GHz.[12] This is a factor of 3 lower power than comparable InP-based LNAs at the same frequency.

Significant increases in $f_T$ and $f_{max}$ have been achieved in InP-based HEMTs by reducing the gate length to less than 100 nm.[14–16] A goal of this work is to develop heterostructures for sub-100-nm InAs-channel HEMTs. In order to maintain good charge control (e.g., minimal short-channel effects) in the scaled devices, it is essential that the gate-to-channel separation also be reduced. An additional advantage of reduced gate-to-channel separation is that the threshold voltage, $V_{th}$, will be closer to 0 V. To quantify this, we performed modeling of $V_{th}$ as a function of sheet density and vertical spacing and compared the results to experimental data.[1] At a density of $2 \times 10^{12}/cm^2$, $|V_{th}|$ decreases from 1.0 V at a separation of 22 nm to 0.5 V for 10 nm, with all in depletion mode. Low $|V_{th}|$ is important because it allows operation at low drain voltage and hence low power dissipation. In addition, low $|V_{th}|$ reduces the gate-to-drain voltage and resulting breakdown phenomena.[17] Additional goals of this study include the elimination of highly reactive

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AlSb from the heterostructures and the addition of $n^+$ cap layers for lower access and contact resistances.

## EXPERIMENTAL

A typical heterostructure is shown in Fig. 1a. Samples were grown by solid-source molecular beam epitaxy (MBE) on a Riber 21T system. The temperature was held constant near 500°C for the AlGaSb buffer, InAs channel, and InAlSb spacer layers. The temperature was decreased (usually to 450°C) for the Te $\delta$-doping, the InAlSb barrier, and the InAs cap layers. The temperature of the GaTe cell was 600°C for all samples reported here. This corresponds to a density of about $2 \times 10^{18}/\text{cm}^3$ at a 1 ML/s growth rate. The Te dose was varied by changing the length of time the stagnant surface was exposed to a GaTe flux (soak time). The growth process was similar to that used for InAs/AlSb transistor structures in the past; more details are given elsewhere.[18] Table I includes a summary of all the samples grown for this study. Hall/van der Pauw transport measurements were made on $5 \times 5$ mm$^2$ squares at room temperature and 0.37 T. Results were confirmed at 1.0 T for selected samples. Some samples were grown for whole-wafer circuit processing. Hence, destructive transport measurements were not possible. For these samples, we report the mobility and sheet density measured by a Lehighton mobility mapping system. For all samples, we also report the resistivity measured by a different Lehighton resistivity mapping system. Atomic force microscopy (AFM) measurements were performed on selected samples to yield root-mean-square (rms) roughness. X-ray diffraction measurements were made on a double-crystal system using Cu $K_\alpha$ radiation. Ultra-low-energy secondary ion mass spectroscopy (SIMS) measurements were conducted using 300 eV $Cs^+$, 500 eV $Cs^+$, and 1,000 eV $Cs^+$ ions.

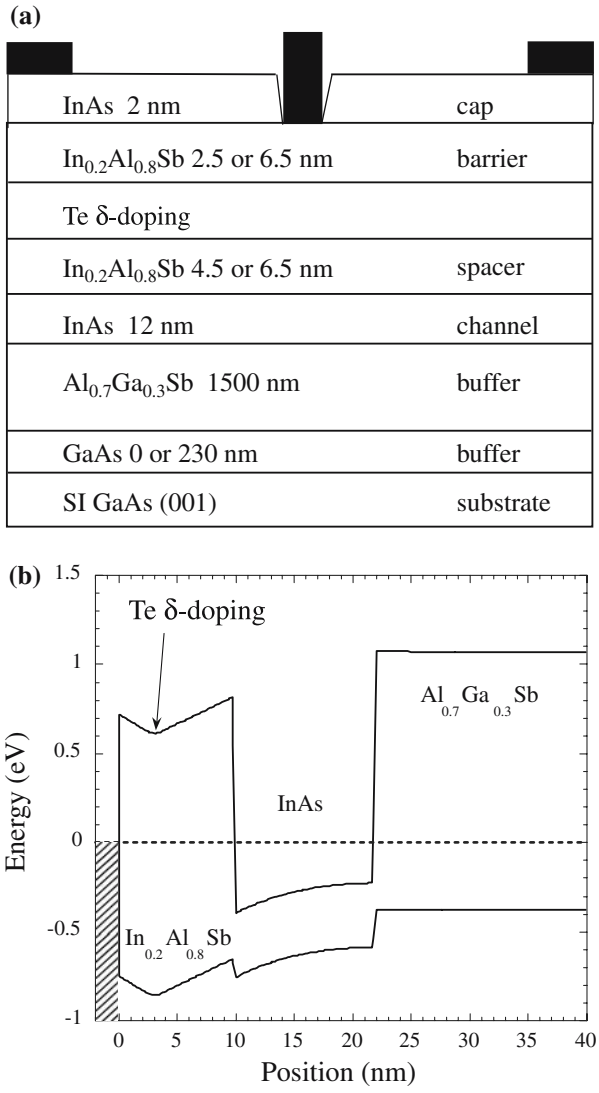


Fig. 1. (a) Cross section of the InAlSb/InAs/AlGaSb HEMT structure and (b) calculated band structure.

## RESULTS AND DISCUSSION

A band diagram of the InAlSb/InAs HEMT structure as obtained from a calibrated density-gradient simulation is shown in Fig. 1b. Both the AlGaSb and InAlSb layers provide a large conduction band offset with respect to the InAs, allowing good confinement of electrons. A significant difference between this structure and our earlier HEMTs[18,19] is that the InAlSb upper barrier replaces InAlAs and AlSb.[20] One reason for this change was to avoid the use of pure AlSb, because Miya *et al.* showed that replacing 20–40% of the Al with Ga in AlGaAsSb greatly reduces oxidation.[21]

The x-ray diffraction data for sample Q is shown in Fig. 2. Peaks are visible for the GaAs substrate, AlGaSb buffer, InAs channel, and InAlSb barrier layers. Assuming the nominal layer thicknesses shown in Fig. 1a (13-nm InAlSb), simulations using RADS software from Bede Scientific yielded a good match to the experimental data for layers of $Al_{0.68}Ga_{0.32}Sb$, $R = 97.9\%$; InAs, $R = 15\%$; and $In_{0.207}Al_{0.793}Sb$, $R = 0\%$, where $R$ is the degree of relaxation. Such fits are not unique, because, for example, other combinations of composition and relaxation of the $Al_xGa_{1-x}Sb$ layer can yield the same Bragg angle. The value of $x = 0.68$ was chosen because it is in reasonable agreement with our nominal value of 0.70 from MBE reflection high-energy electron diffraction (RHEED) oscillation calibrations and because the corresponding relaxation value is close to what we have found in the past for pure AlSb layers of similar thicknesses on GaAs.[18] If $R > 0$ is assumed for the $In_yAl_{1-y}Sb$ layer, then larger values of $y$ are required and are not consistent with our nominal value. For the InAs layer, the experimental peak position can also be matched for $R = 0\%$ if 2% Sb cross-contamination is assumed. Our results suggest that the InAlSb and

**Table I. Growth Parameters and Room-Temperature Transport Results for All Samples: $R_{SH1}$ is the Sheet Resistance from Room-Temperature Hall/Van Der Pauw Measurements (Samples A-F and I-K) or a Lehighton Mobility Mapper (Samples G, H, and L-Q); and $R_{SH2}$ is the Sheet Resistance from a Lehighton Resistivity Mapper. The $n^+$ Cap Layer is 20-nm InAs Doped with $\sim 1 \times 10^{19}/cm^3$ Te**

| Sample | Spacer (nm) | Upper Bar (nm) | GaTe Soak (sec) | Soak Temp. (°C) | Sb Flux During δ Dop. | GaAs Buffer | n+ Cap | $n_s$ ($\times 10^{12}$ cm$^{-2}$) | $\mu_{300\ K}$ (cm$^2$/V s) | $R_{SH1}$ (Ω/□) | $R_{SH2}$ (Ω/□) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | 4.5 | 2.5 | 0 | — | — | Y | N | 0.3 | 12,800 | 1600 | 650 |
| B | 4.5 | 2.5 | 33 | 450 | Y | Y | N | 1.6 | 20,000 | 200 | 176 |
| C | 6.5 | 2.5 | 33 | 450 | Y | Y | N | 1.4 | 23,500 | 197 | 184 |
| D | 6.5 | 2.5 | 30 | 450 | Y | N | N | 1.4 | 21,300 | 212 | 174 |
| E | 6.5 | 2.5 | 30 | 500 | Y | N | N | 1.2 | 20,000 | 256 | 330 |
| F | 6.5 | 2.5 | 30 | 450 | N | N | N | 1.2 | 18,100 | 289 | 218 |
| G | 6.5 | 2.5 | 30 | 450 | Y | N | N | 1.4 | 25,000 | 178 | 232 |
| H | 6.5 | 2.5 | 30 | 450 | Y | N | N | 1.4 | 24,000 | 186 | 228 |
| I | 6.5 | 2.5 | 30 | 450 | Y | N | Y | — | — | — | 78 |
| I | 6.5 | 2.5 | 30 | 450 | Y | N | Y | 2.0 | 23,200 | 135 | — |
| J | 6.5 | 2.5 | 50 | 470 | Y | N | N | 2.4 | 21,100 | 125 | 171 |
| K | 6.5 | 2.5 | 50 | 430 | Y | N | N | 2.4 | 18,400 | 144 | 195 |
| L | 6.5 | 6.5 | 30 | 450 | Y | N | N | 1.6 | 20,100 | 188 | 177 |
| M | 6.5 | 6.5 | 30 | 450 | Y | N | Y | — | — | — | 74 |
| N | 6.5 | 6.5 | 30 | 450 | Y | N | Y | — | — | — | 78 |
| O | 6.5 | 6.5 | 30 | 450 | Y | N | N | 1.5 | 19,700 | 211 | 160 |
| P | 6.5 | 6.5 | 30 | 450 | Y | N | N | 1.1 | 23,100 | 249 | 243 |
| Q | 6.5 | 6.5 | 30 | 450 | Y | N | N | 0.9 | 22,200 | 327 | 326 |

InAs layers are nearly coherent with respect to the relaxed AlGaSb buffer layer, with the InAs in tension (1.1% mismatch) and the InAlSb in compression (1.3% mismatch).

The depth resolution of conventional SIMS can be poor due to intermixing induced by the high-energy ions. Using lower ion energies can reduce this problem. Exploiting this strategy, we analyzed sample I with SIMS and found the δ-doped Te profile full-width at half-maximum (FWHM) decreased from 4.7 nm to 3.5 nm when the ion energy was reduced from 1,000 eV to 500 eV. A further reduction to 300 eV resulted in only a small change in width to 3.3 nm. On that basis, we conclude that the 300 eV profile should be a good approximation to the real distribution. This profile is shown in Fig. 3. The $y$-axis calibration is based upon our expected total dose of Te, which was derived from transport measurements on thick layers of GaAs(Te). The profile is relatively symmetric suggesting that diffusion and not segregation of Te in InAlSb dominates. The Te concentration drops by over two orders of magnitude from the peak to the top interface with the InAs quantum well where the value is near $2 \times 10^{16}/cm^3$. Throughout most of the quantum well, background concentrations in the mid-$10^{15}/cm^3$ range are observed. Although Te may suffer from significant desorption, segregation, and diffusion for some materials and growth conditions,[22,23] the results of this study suggest that it can be a suitable dopant in InAlSb. These results are comparable to the Si δ-doping of InAlAs, often used for InP HEMTs, where SIMS using 1,000-eV ions yielded a FWHM near 5 nm.[24]

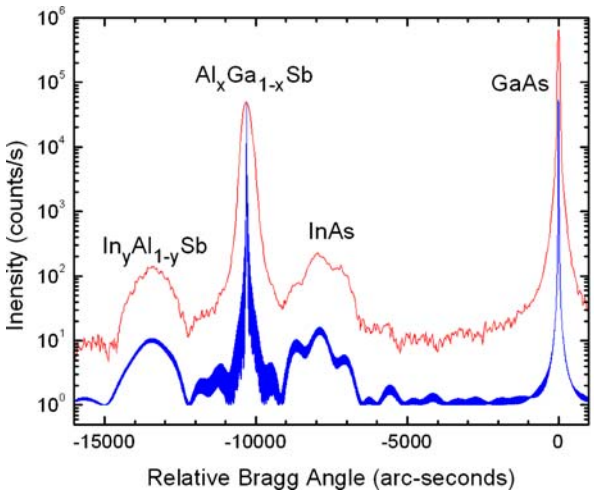


Fig. 2. Double-crystal x-ray diffraction of sample Q near the (004) reflection. The lower trace is a simulation (refer to text).

In Fig. 4, we plot the room-temperature mobility versus the sheet carrier density for 12 samples (Table I). The intentionally doped samples have mobilities between 18,000 and 25,000 cm$^2$/V s and densities between 1.2 and $2.4 \times 10^{12}/cm^2$. The sheet density can be controlled by varying the soak time of the Te δ doping. Several other trends can also be observed from Table I. Three samples were grown with a 230-nm GaAs buffer layer. This should provide a smoother surface for the subsequent deposition of the AlGaSb buffer layers. The data show no apparent difference in the mobility and density for samples with and without the GaAs buffer layer. As

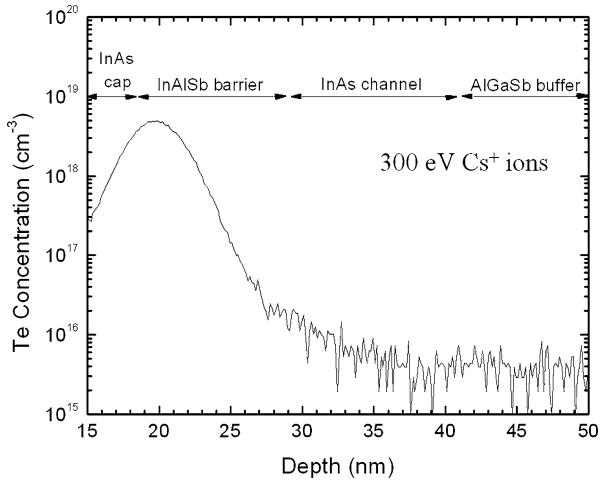


Fig. 3. Low-energy SIMS showing Te $\delta$ doping in InAlSb.

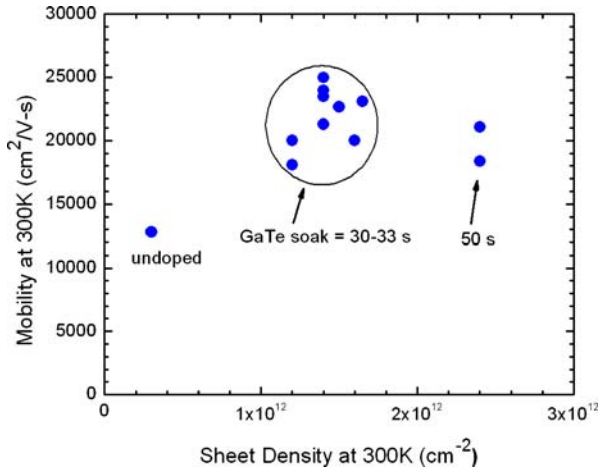


Fig. 4. Room-temperature mobility as a function of sheet density. The GaTe cell temperature was fixed and the soak times were varied as indicated. All samples included here were capped with 2-nm undoped InAs. Note that samples P and Q were grown after a vent and reloading of the GaTe source, resulting in a change in the GaTe flux; they are not included in this plot.

mentioned above, the growth temperature was typically reduced from 500°C to 450°C for the Te $\delta$-doping. The goal was to reduce Te segregation and diffusion. Similar changes in growth temperature are sometimes used for Si-doped InP-based HEMTs.[25,26] To test the importance of the growth temperature, $\delta$-doping substrate temperatures of 430°C, 470°C, and 500°C were also used. As shown in Table I, there is no significant effect on the mobility or density. This is encouraging in that precise control of the growth temperature is not necessary. [In previous work on InAs/AlSb quantum wells, we found that high mobilities could be achieved over a relatively large range of growth temperatures for the InAs (~470–520°C).] Our normal procedure was to leave the Sb shutter open during deposition of GaTe. For sample F, we closed the Sb shutter but observed no significant differences. Our standard spacer thickness was 6.5 nm, but good mobility (20,000 cm$^2$/V s) was achieved for 4.5 nm (sample B). The upper barrier thickness was either 2.5 or 6.5 nm with the lower value providing a better aspect ratio for very short gates, but the higher value probably yielding lower gate leakage currents (as has been demonstrated for 70-nm InGaAs-channel HEMTs).[27]

We recently reported transistor characteristics for a device with the structure of Fig. 1a (6.5-nm spacer and 2.5-nm upper barrier) and a 350-nm gate length. The devices have a DC transconductance of 1 S/mm and an intrinsic $f_T$ of 95 GHz,[28] a result consistent with other InAs HEMTs at comparable gate lengths.[1] The significance of this result is that the structure contains no AlSb,[29] and the distance from the gate to the channel is only 9 nm. For comparison, the gate-to-channel separations for 100-nm InAs HEMTs were 14–19 nm.[3,10,30] We note that a study of InP HEMTs demonstrated good microwave performance if the gate length was greater than the sum of the gate-to-channel separation and the channel thickness.[16] For our structures, the sum is 19–25 nm. The scaling properties may be different for InAs HEMTs. Experimental work to achieve sub-100-nm gates is in progress in our laboratory.

Low sheet resistance, $R_{SH}$, is desirable for good RF performance. The $R_{SH}$ values as low as 100 Ω/sq can be achieved by high channel doping (e.g., $n_s \sim 3 \times 10^{12}$/cm$^2$, $\mu \sim 20{,}000$ cm$^2$/V s).[18] However, high values of $n_s$ can result in large $V_{th}$.[1] To address this dilemma, we are investigating a recessed-gate approach with a thick $n^+$ cap layer. We initially grew $n^+$ InAs caps on top of our standard InAlAs barrier layers. There is a large lattice mismatch between the InAlAs ($a_o$ = 5.9 Å) and the other layers ($a_o \sim 6.1$ Å). As expected, during InAlAs growth, the RHEED pattern becomes spotty, indicating three-dimensional growth. Although we were able to successfully cap the InAlAs with 2-nm InAs, we could not do so with 20-nm $n^+$ InAs. These $n^+$ caps were very rough and did not result in good device properties. By changing the upper barrier to $In_{0.20}Al_{0.80}Sb$, which has a lattice constant of 6.20 Å and is coherently strained, we were able to routinely grow 20-nm $n^+$ InAs caps with good surface morphology and etching properties. Our AFM rms roughness values ($5 \times 5$ $\mu$m$^2$ area) are near 1 nm for as-grown samples with and without the $n^+$ caps as well as for samples after removal of the $n^+$ cap. As shown in Table I, we obtained as-grown sheet resistances of 74–78 Ω/sq. For sample I, we performed transport measurements after removing the $n^+$ cap with a chemical etch. The mobility was good (23,200 cm$^2$/V s); the sheet density ($2.0 \times 10^{12}$/cm$^2$) was higher than usual for this GaTe soak time, probably because of surface effects.[31] The device properties are under investigation and will be reported elsewhere.

Another group recently fabricated high-performance transistors with $n^+$ InAs caps on InAlAs/AlSb barriers.[17] The InAlAs passivates the highly reactive AlSb, which enables the use of a gate recess process. Another reason for using InAlAs barriers is that, based upon the band structure, they should provide a barrier for holes generated in the channel by impact ionization, hence reducing gate leakage currents. Our preliminary measurements on devices with InAlSb/InAs/AlGaSb heterostructures suggest relatively low leakage currents may be possible without the InAlAs barrier.

The work described here involved Te-doped structures. We have also grown structures using a 1.2-nm InAs(Si) doping layer[32,33] as well as InAlSb upper barriers, AlGaSb buffer layers, and small gate-to-channel separations (12 nm). Some samples also included a 20-nm $n^+$ InAs cap. The values of mobility, density, and rms roughness were comparable to what we report here for Te-doped structures. All of the Si-doped structures contained a total of 57 nm of AlSb above and below the channel, but we see no reason the AlSb could not be totally eliminated as we have done for the Te-doped structures.

## SUMMARY

We investigated heterostructures for InAs-channel HEMTs containing $Al_{0.7}Ga_{0.3}Sb$ buffer layers and $In_{0.2}Al_{0.8}Sb$ upper barriers with Te $\delta$-doping. The SIMS measurements indicate that very little Te is diffusing into the channel. The carrier density can be controlled by the GaTe soak time. Room-temperature mobilities range from 18,000 to 25,000 $cm^2/V$ s. The channel thickness is 12 nm and the gate-to-channel separation ranges from 7 to 13 nm. These values should allow scaling to sub-100-nm gate lengths. X-ray diffraction measurements show that the $In_{0.2}Al_{0.8}Sb$ is coherently strained. The AFM measurements indicate relatively smooth surfaces of the standard structures as well as samples with a 20-nm $n^+$-InAs cap. The use of $n^+$ caps should result in HEMTs that simultaneously have low sheet resistance (<100 Ω/sq) and moderate sheet carrier density ($\sim 1 \times 10^{12}/cm^2$). The absence of reactive AlSb is expected to improve the reliability and manufacturability of the HEMTs.

## ACKNOWLEDGEMENTS

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