High mobility p-channel HFETs using strained Sb-based materials

J.B. Boos, B.R. Bennett, N.A. Papanicolaou, M.G. Ancona, J.G. Champlain, R. Bass and B.V. Shanabrook

Antimonide-based p-channel HFETs with a 0.25 μm gate length have been fabricated with an InAlSb/AlGaSb barrier and a strained $In_{0.41}Ga_{0.59}Sb$ quantum well channel. The modulation-doped material exhibits a Hall mobility of 1020 cm^2/V s and a sheet density of 1.6×10^{12} cm^{-2}. The devices have a maximum DC transconductance of 133 mS/mm and an f_T and f_{max} of 15 and 27 GHz, respectively. These values are the highest reported to date for this material system.

Recently, there has been considerable interest in the potential of III-V FET materials for advanced logic applications which could significantly enhance digital circuit functionality and extend Moore's Law [1]. Sb-based HFETs are attractive candidates for these high-performance logic circuits owing to their high-speed and low-power potential. Sb-based complementary circuits needed for this technology will require p-channel HFETs with high hole mobility. For this purpose, the $In_xGa_{1-x}Sb$ alloy system is attractive since the binary endpoints have the highest bulk hole mobilities of any III-V compound and a significant valence band barrier to enable quantum confinement [2, 3]. This potential can be enhanced by using strain to produce advantageous band splitting as has been exploited to great effect in Si and SiGe pMOSFETs. As work in this direction, we report on the fabrication and characteristics of Sb-based HFETs with an InAlSb/AlGaSb barrier, a strained, high-mobility, p-type $In_{0.41}Ga_{0.59}Sb$ quantum well channel, and no highly-reactive AlSb material within the structure.

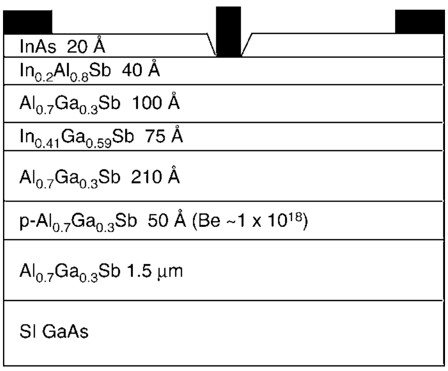

Fig. 1 *Starting MBE material structure*

The Sb-based HFET material was grown by molecular beam epitaxy on a semi-insulating (100) GaAs substrate. A 1.5 μm undoped $Al_{0.7}Ga_{0.3}Sb$ buffer layer was used to accommodate the 8% lattice mismatch. A cross-section of the device, showing the material layer design, is given in Fig. 1. Details of the growth procedures will be described elsewhere [4]. Because the $In_{0.41}Ga_{0.59}Sb$ channel layer is grown epitaxially on the relaxed AlGaSb buffer, it will be in a state of biaxial compressive strain. For this particular composition, the strain is about 2%. Modulation doping is achieved using a 5 nm Be-doped $Al_{0.7}Ga_{0.3}Sb$ layer below the channel. The inverted doping scheme was chosen to enhance the capability for future scaling to ultra-thin gate-channel separations. A band diagram of the structure is shown in Fig. 2, where the $Al_{0.7}Ga_{0.3}Sb/In_{0.41}Ga_{0.59}Sb$ valence band offset is 400 meV and the calculated heavy and light hole ground state energies in the well are 40 and 212 meV, respectively, below the valence band edge. The band diagram and energy levels were obtained using an 8×8 k · p method as implemented in the 'next-nano[3]' program that includes the effects of non-parabolicity and strain. The room-temperature Hall mobility and sheet carrier concentration of the starting material for the HFETs reported here were 1020 cm^2/V s and 1.6×10^{12} cm^{-2}, respectively. In other samples, this design has yielded room temperature Hall mobilities as high as 1500 cm^2/V s [4].

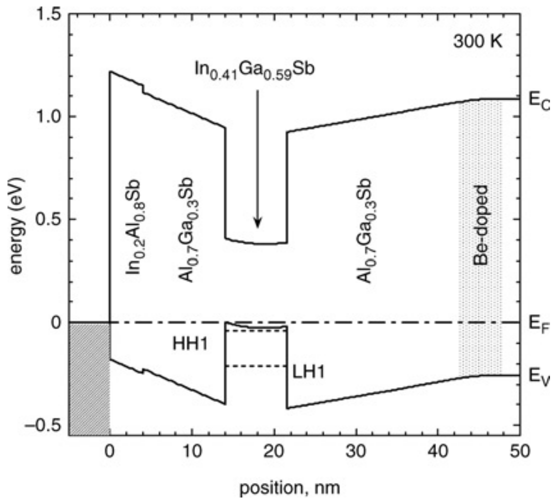

Fig. 2 *p-Channel HFET energy-band diagram*

The HFETs were fabricated using Pd/Pt/Au source and drain ohmic contacts which were formed by heat treatment on a hot plate. A TiW/Pt/Au Schottky-gate was then formed using PMMA e-beam lithography and lift-off techniques. The selective etch properties of the InAlSb barrier enabled the use of a gate recess etch through the InAs cap layer prior to gate metal definition. After a Cr/Au overlay metal pattern was formed, device isolation was achieved by wet chemical etching. With this etch, a gate air bridge was formed which extends from the channel to the gate bonding pad.

The drain characteristics obtained for a HFET with a 0.25 μm gate length are shown in Fig. 3. The low-field source-drain resistance at $V_{GS} = -0.4$ V is 7.6 Ω mm. The contact resistance was estimated to be 2 Ω mm using TLM measurements. The dependence of the transconductance on the gate voltage is shown in Fig. 4. At $V_{DS} = -2.5$ V, a maximum transconductance of 133 mS/mm is observed at $V_{GS} = -0.05$ V, which is the highest reported for this material system. The gate-source diode I-V characteristic exhibits good rectification and a gate current of 2.5 A/cm^2 at a gate-source bias of 1 V. The use of an MIS approach to reduce the gate current is currently under investigation. A threshold voltage of 0.14 V was measured at $V_{DS} = -2$ V. The subthreshold slopes at $V_{DS} = -0.05$ and -2 V were 114 and 170 mV/dec, respectively. These values are elevated owing to a source-drain leakage current that is also currently under investigation. The *S*-parameters of the HFETs were measured on-wafer from 1 to 40 GHz. Based on the usual 6 dB/octave slope, a maximum f_T of 15 GHz and f_{max} of 27 GHz were obtained. These values are the first reported for Sb-based p-channel HFETs. The f_{max} should improve with the implementation of a low-gate-metal-resistance T-gate structure. Using a simplified equivalent circuit, a microwave transconductance and output conductance of 130 and 6.5 mS/mm were obtained, respectively, at $V_{DS} = -3$ V and $V_{GS} = 0$ V. The gate leakage current at this bias condition was 500 nA. Further improvements in high-speed, low-voltage performance should be possible with a decrease in gate length and a reduction of the contact and access resistances.

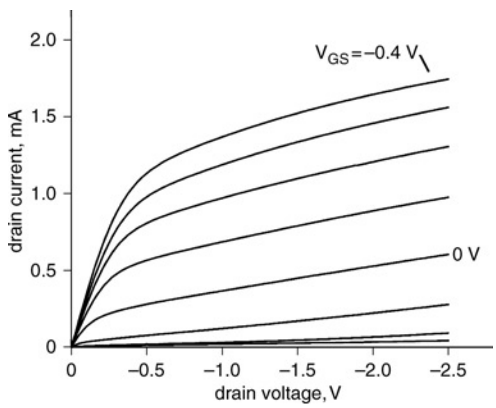

Fig. 3 *HFET drain characteristics*

L_G = 0.25 μm, L_{DS} = 1.0 μm, W_G = 28 μm, V_{GS} = 0.1 V/step

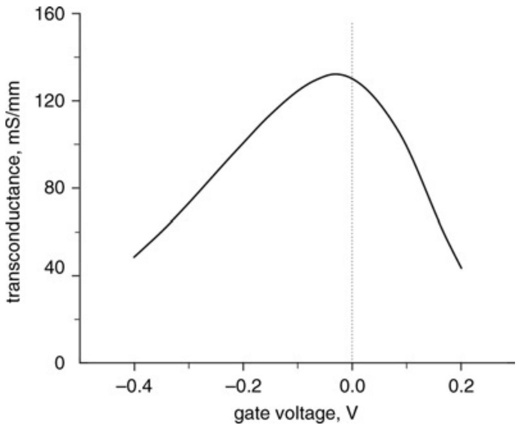

Fig. 4 *HFET transconductance against gate voltage at $V_{DS} = -2.5$ V*

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