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Demonstration of high-mobility electron and hole transport in a single InGaSb well for complementary circuits

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ABSTRACT

Heterostructures consisting of an InGaSb quantum well situated between AlGaSb barriers were grown by molecular beam epitaxy. Calculations indicate a type-I band structure with substantial valence and conduction band offsets that can allow for the confinement of either electrons or holes in the InGaSb. Quantum wells with n-type conduction were achieved using modulation doping, with Te located in the barrier above the quantum well. A set of barrier layers was found which resulted in a sample with an $In_{0.2}Ga_{0.8}Sb$ quantum well that exhibited an electron mobility of 3900 $cm^2/V\,s$ as grown. After removal of upper barrier layers including the Te by selective etching, the conductivity switched to p-type, with hole mobilities near 800 $cm^2/V\,s$. This design could allow the integration of low-power n- and p-channel field-effect transistors for complementary logic applications.

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1. Introduction

Complementary metal–oxide–semiconductor (CMOS) design is the key technology of mainstream digital electronics that allows ultra-high levels of integration to be achieved by greatly reducing power dissipation. From an implementation standpoint, CMOS is superbly well served by the Si/SiO_2 material system. It provides nearly matching mobilities for electrons and holes and the ability to withstand high-temperature processing, allowing one to fabricate the requisite n- and p-channel transistors within a single layer of Si simply by doping the source/drain regions (as contacts) and channels (for threshold control) appropriately. Unfortunately, the III–V compound semiconductors are nowhere near as suitable a match for CMOS. Their electron and hole mobilities are markedly different, and a requirement of low-temperature processing greatly limits the strategies available for doping. Nevertheless, the tremendous potential benefits for power dissipation and speed have motivated various efforts aimed at overcoming these challenges and exploring the feasibility of III–V CMOS.

The focus of the present paper is on demonstrating a Si-like situation in which high-quality electron and hole transport both are achieved within a single III–V layer. To achieve this goal, one must design a single quantum well/barrier heterostructure which (1) provides a quantum well with high hole and electron mobilities, (2) provides good confinement for both the electrons and holes, and (3) permits a doping scheme that can easily allow one to select which areas of the structure are to be n- and p-channel. In this paper, we demonstrate a scheme that achieves all three of these objectives using a single InGaSb channel.

2. Heterostructure design

Earlier, several groups investigated the integration of n- and p-channel field-effect transistors (FETs). In 1989, Kiehl and colleagues at IBM designed and fabricated a single heterostructure that included both n- and p-channel GaAs layers with AlGaAs barriers, and demonstrated p-channel FETs operating at 77 K [1]. A decade later, a group at Motorola formed adjacent n- and p-channel GaAs FETs using ion implantation and demonstrated digital circuits [2]. More recently, Leuther et al. demonstrated room-temperature ring oscillators using complementary n- and p-FETs with separate InGaAs channels and Al(Ga)As barriers grown in a single heterostructure [3]. Tsai et al. fabricated n- and p-channel FETs using InGaAs channels and InGaP barriers [4].

It is desirable that the material for the n- and p-channels and barriers have similar lattice constants to avoid three-dimensional

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growth and strain-induced misfit dislocations. The heterostructures with GaAs and InGaAs channels discussed above have lattice constants near 5.7 Å. An alternative is to use materials with lattice constants of 6.1 Å and greater, namely GaSb, InSb, AlSb, InAs, and related alloys. In general, these materials have smaller bandgaps, with the potential for lower power consumption [5,6]. In the last few years, they have been exploited for low-power, high-frequency, n-channel FETs. Low-noise amplifiers operating at frequencies of 10–100 GHz have been reported. In these analog circuits, the narrow bandgap and high mobility result in 3–10 times lower power consumption than is seen with comparable InP- or GaAs-based circuits [6]. In 1990, Longenbach et al. proposed a complementary FET technology that would use InAs for the n-channel and GaSb for the p-channel [7]. Yoh et al. fabricated n-InAs-channel and p-GaSb-channel FETs from a single heterostructure, and achieved FETs operating at 77 K [8,9]. In related work, Yang et al. demonstrated an FET structure with a composite InAs/GaSb well. By varying the gate voltage, they were able to switch the 2D carrier type from electrons to holes [10].

More recently, there have been various III–V efforts attempting to provide improved barrier technologies [11] and to raise the hole mobilities in III–V semiconductors. The challenge with respect to mobility is readily seen in the bulk mobilities. For example, at room temperature GaAs has an electron mobility of 8000 $cm^2/V\,s$ while the hole mobility is only 400 $cm^2/V\,s$. In the case of InAs the difference is even greater with the respective values being 33,000 and 460 $cm^2/V\,s$. Because the antimonide-based semiconductors (i.e., InSb, GaSb, and their alloys) have the highest bulk hole mobilities of all III–V semiconductors, efforts to improve hole mobility have been focused on these materials. We recently demonstrated the use of compressive strain to achieve significant enhancement of hole mobility using GaSb channels with AlAsSb barriers. The strain and confinement lift the degeneracy of the heavy- and light-hole valence bands, resulting in a decrease in average effective mass and an increase in mobility. Room-temperature mobilities as high as 1350 $cm^2/V\,s$ were achieved [12]. We also investigated strained InGaSb channels on AlGaSb buffer layers and achieved Hall mobilities as high as 1500 $cm^2/V\,s$ [13]. With $In_{0.4}Ga_{0.6}Sb$ as the channel in a p-FET, a maximum transconductance of 133 mS/mm was achieved [14]. For a 200 nm gate length, the cutoff frequency, f_T, was 19 GHz, and the maximum oscillation frequency, f_{max}, was 34 GHz [15]. Lower access resistance is expected to lead to improvements in both DC and RF performance. Another research team investigated InSb-channel FETs with InAlSb barriers [16]. They achieved room-temperature mobilities as high as 1230 $cm^2/V\,s$. Their devices exhibited a maximum transconductance of 510 mS/mm. For a 40 nm gate length, an f_T of 140 GHz was obtained. The significance of these results is displayed in Fig. 1 where we compare the hole mobilities achieved for antimonide-based quantum wells with the best results from the literature for arsenide-based quantum wells.

Based upon the successful strain enhancement of hole mobilities in the antimonides, we investigated InGaSb as a channel material for both electrons and holes. In Fig. 2a, we plot the calculated band structure for a 10 nm quantum well of $In_{0.2}Ga_{0.8}Sb$ clad with $Al_{0.8}Ga_{0.2}Sb$ where the calculations were performed using the Nextnano simulation program [17]. The calculation assumed no extrinsic doping of the heterostructure. The figure shows a 0.4 eV valence band offset, which should be sufficient to confine holes in the InGaSb. The position of the Fermi level indicates that the structure should be p-type at zero bias. Our experimental results were consistent with this: hole sheet densities near $7 \times 10^{11}/cm^2$ for undoped InGaSb quantum wells [13]. (Undoped quantum wells of GaSb clad with AlAsSb also had

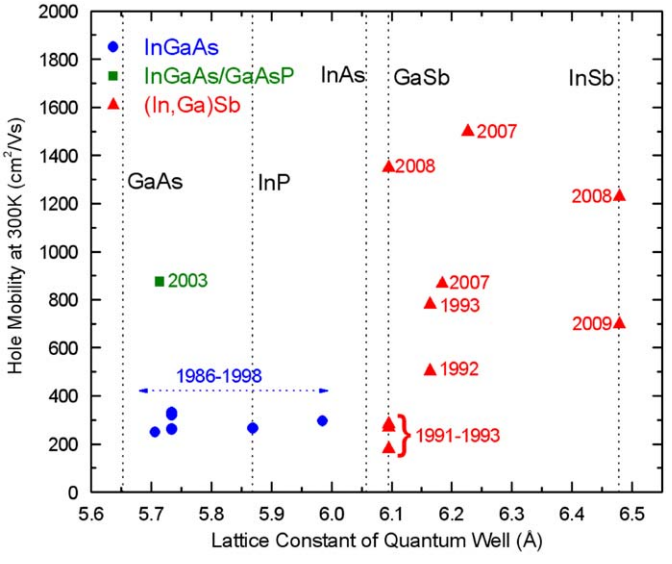

Fig. 1. Room-temperature hole mobility versus lattice constant for quantum wells formed by III–V compound semiconductors. The quantum well strain and sheet carrier density vary considerably amongst the samples. Data are from the following references: InGaAs [22–27], InGaAs/InGaP [28], GaSb [8,12,29], InGaSb [13,30], and InSb [16,31].

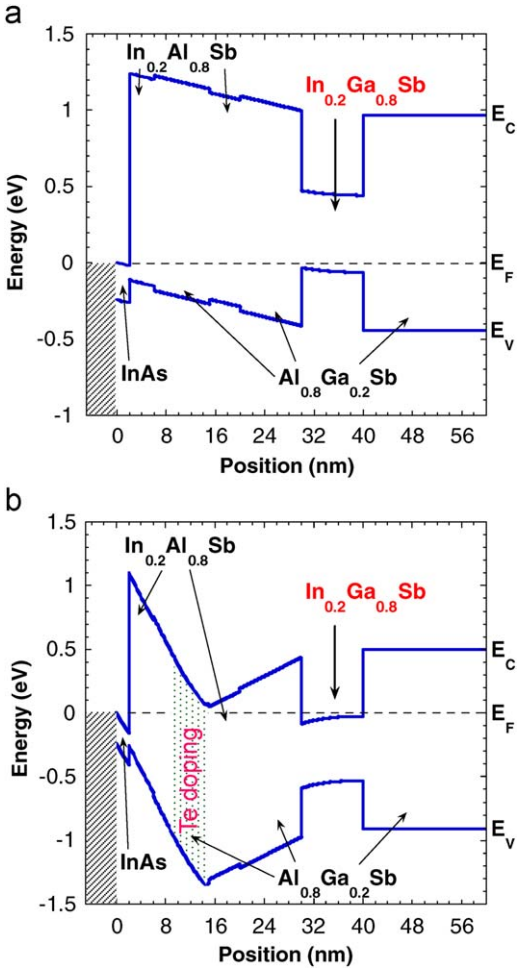

Fig. 2. Calculated energy band diagrams for undoped (a) and Te-doped (b) InGaSb/AlGaSb quantum well structures.

similar hole densities [12].) Fig. 2a further indicates that the InGaSb/AlGaSb structure has a large conduction band offset, allowing for the confinement of electrons in the InGaSb well. When, as shown in the band diagram in Fig. 2b, the same structure has n-type (Te) doping introduced above the quantum well, the Fermi level indicates the structure should be n-type at zero bias, with a conduction band offset of 0.5 eV. This structure was not studied experimentally heretofore.

3. Experimental procedures

To investigate InGaSb quantum wells in detail, we used solid-source molecular beam epitaxy (MBE) to grow a series of Te-doped heterostructures similar to the one depicted in Fig. 2b. Epilayers are grown on semi-insulating GaAs substrates, using a Riber Compact 21T system equipped with valved As and Sb cracking cells. After oxide desorption near 600 °C, the temperature is lowered to 525 °C and a 1.5 μm buffer layer of $Al_{0.8}Ga_{0.2}Sb$ is grown. This buffer layer is almost fully relaxed, relieving the 8% lattice mismatch between the substrate and epilayers. The growth temperature is then lowered to 450 °C, and the $In_xGa_{1-x}Sb$ channel is grown, with x varying from 0 (GaSb) to 0.35. This is followed by $Al_{0.8}Ga_{0.2}Sb$ and $In_{0.2}Al_{0.8}Sb$ barrier layers (including Te doping from a GaTe source), and an InAs cap. Hall-van der Pauw transport measurements were made on $5\times5\,mm^2$ squares at 300 K, using fields of 0.37, 0.55, and 1.0 T. Several samples were grown with what was nominally enough Te doping to compensate the p-type background and give electrons in the well. In each case, the sample was highly resistive ($>100{,}000\,\Omega/\square$). We eventually achieved n-type conduction in the well by using extremely high levels of Te doping, with activation efficiencies of only about 3%. Two other groups also reported using very high concentrations of donor atoms to achieve n-type doping for GaSb [18] and InGaSb [19] FET structures. We speculate that a high density of deep traps exists in either the well or barrier material.

4. Results and discussion

In Fig. 3, we plot the electron mobility as a function of InSb mole fraction, x, in $In_xGa_{1-x}Sb$ for five samples, labeled A–E. The sheet concentrations were $4–5\times10^{11}/cm^2$. The hole mobilities for $In_xGa_{1-x}Sb$ from our earlier work are also included in Fig. 3 [13]. For all samples, the buffer layer was 1.5 μm $Al_yGa_{1-y}Sb$ with y=0.70–0.80. As x increases, the lattice constant of the $In_xGa_{1-x}Sb$ grows, resulting in channels with increasing compressive strain. For example, the strains for $In_{0.2}Ga_{0.8}Sb$ and $In_{0.4}Ga_{0.6}Sb$ are 0.73% and 1.98%, respectively. If the lattice mismatch is too large, however, misfit dislocations will form to relieve the strain. We see that the highest hole mobilities ($\sim1000\,cm^2/V\,s$) are obtained for alloys with $x\sim0.4$. (At this composition, mobilities as high as $1500\,cm^2/V\,s$ were achieved by varying the well thickness and growth procedures [13].) For electrons, however, the highest mobility ($8400\,cm^2/V\,s$) is achieved for sample C with x=0.2. Sample E, with x=0.35, has a mobility of only $2000\,cm^2/V\,s$.

As discussed earlier, it is desirable to have a single heterostructure that includes both the n- and p-channel FETs. In previous work with GaAs, InGaAs, and InAs/GaSb channels, separate layers were grown for the n- and p-channels. In the antimonide system studied here, it may be possible to do as in standard Si technology and use the same channel for both the n- and p-FETs. Based on the results in Fig. 3, we selected $In_{0.2}Ga_{0.8}Sb$ as the channel material. The design is illustrated in Fig. 4, and corresponds to the band structures in Fig. 2. With sufficient Te doping, the structure will be n-type as grown, and an n-FET can be

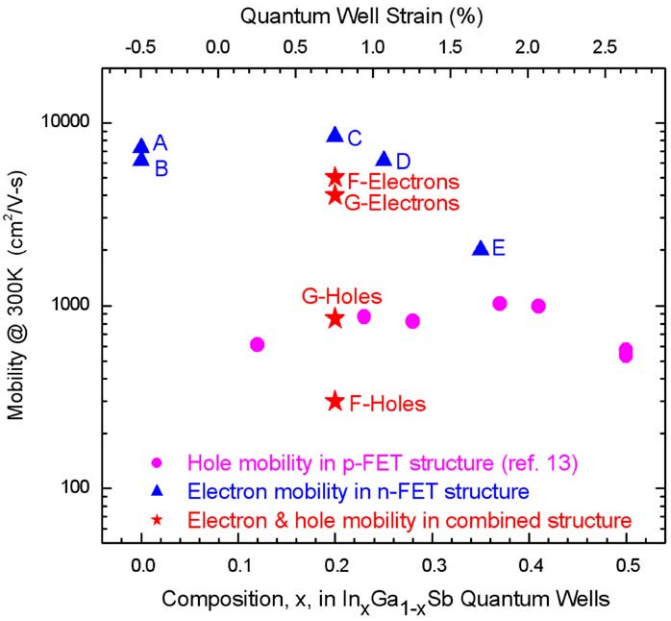

Fig. 3. Electron mobility (this study) and hole mobility [13] of $In_xGa_{1-x}Sb$ as a function of composition. The biaxial strain in the InGaSb layers is given by the top axis, with positive values indicating compressive strain and negative values indicating tensile strain.

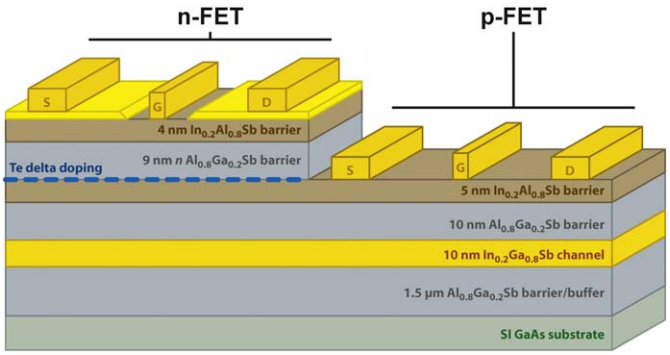

Fig. 4. Cross-section of InGaSb-channel FET structure. As-grown (left side), will be n-type. After removal of the top layers (right side), the structure will be p-type. Positions of the source (S), gate (G), and drain (D) contacts are also shown.

fabricated as shown on the left side. The right side of the structure (Fig. 4) has been etched to remove the top layers including the Te doping. Since similar undoped structures are normally p-type, fabrication of a p-FET on the etched material should be possible. For higher hole density, Be doping below the InGaSb well could also be added. The thickness of the upper barrier layers could be reduced to decrease the gate-to-channel thickness and facilitate FETs with very short gate lengths. Incorporation of suitable dielectrics could permit extremely thin barrier layers with low leakage currents.

Following the design concept of Fig. 4, we grew several such structures. The first sample, F, did not include the 5 nm InAlSb layer immediately below the Te delta doping. The electron mobility was $5000\,cm^2/V\,s$ (see Fig. 3). After removal of the top layers by wet chemical etching, the quantum well switched to p-type as desired, but the mobility was only about $300\,cm^2/V\,s$. A similar result was obtained when the upper layers were removed from sample C. With addition of 5 nm InAlSb before the Te doping (sample G) the hole mobility improved (Fig. 3). The transport measurements yielded an electron mobility of

3900 $cm^2/V\,s$ and a density of $0.9\times10^{11}cm^{-2}$ as grown. After removal of about 14 nm of material, the sample was p-type with a hole density of $1.0\times10^{11}cm^{-2}$ and a mobility of 820 $cm^2/V\,s$. Removal of an additional 2 nm of material resulted in little change: $0.9\times10^{11}cm^{-2}$ and 760 $cm^2/V\,s$. The improvement of hole mobility from sample F to sample G could result from there being less scattering from surface states of InAlSb compared to AlGaSb. The relatively low sheet carrier densities do not necessarily imply low current drive. Advanced designs including heavily doped cap layers and selective regrowth could be used to emulate Si-based CMOS technology.

The hole mobility value for sample G is comparable to single p-type quantum wells. The electron mobility is about a factor of two lower than single n-type quantum wells. Compared to earlier work on complementary III–V FETs [3,4], the hole mobility we achieved is a factor of two to four higher. To our knowledge, this is the first demonstration using the same channel for the n- and p-type III–V quantum wells. It may be possible to achieve higher hole mobilities without sacrificing electron mobility by, for example, reducing the thickness of the quantum well and possibly increasing the InSb mole fraction [13].

A similar approach could also be used for other compositions of $In_xGa_{1-x}Sb$. Delhaye et al. used graded buffer layers on InP substrates to achieve n-channel-$In_{0.5}Ga_{0.5}Sb$ quantum wells with room-temperature mobilities of 19,000 $cm^2/V\,s$ [19]. No corresponding p-channel work has been reported. Datta et al. investigated n-channel-InSb FETs, and achieved mobilities of 25,000 $cm^2/V\,s$ with excellent high-frequency FET performance [20]. The same group also achieved p-InSb-channel FETs as discussed earlier [16]. Ultimately, which of the antimonide-based materials turns out to be best suited for complementary logic circuit technology will depend not just on the electron and hole mobilities, but also on a host of other factors such as scalability, contact resistance, drive and leakage currents, integrability with oxides/dielectrics, and enhancement-mode capability [21].

5. Summary

In summary, we have demonstrated MBE-grown single quantum wells of GaSb and InGaSb with high electron mobilities can be achieved via modulation doping with Te. With appropriate selection of barrier materials, quantum wells of strained $In_{0.2}Ga_{0.8}Sb$ can be n-type as grown, and, after removal of upper layers by selective etching, will switch to p-type with a hole mobility near 800 $cm^2/V\,s$. Such a structure could be the basis of a low-power III–V CMOS, with the same InGaSb layer used as the channel in both n- and p-FETs. Future goals will include the demonstration of enhancement-mode n- and p-channel FETs with low contact resistance, and the incorporation of suitable dielectrics under the gate.

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