Journal of ELECTRONIC MATERIALS, Vol. 39, No. 10, 2010
DOI: 10.1007/s11664-010-1295-0

AlGaSb Buffer Layers for Sb-Based Transistors

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InAs quantum wells can serve as the channel for high-electron-mobility transistors. Structures are typically grown on semi-insulating GaAs substrates with 1.5 μm to 3.0 μm buffer layers of AlSb and AlGaSb accommodating the lattice mismatch. We demonstrate that high electron mobility in the InAs (>20,000 cm^2/V s at 300 K) and smooth surfaces can be achieved with $Al_{0.8}Ga_{0.2}Sb$ buffer layers as thin as 600 nm, grown at rates of 1.5 monolayers/s to 2.0 monolayers/s. The use of thinner buffer layers reduces molecular beam epitaxial growth time and source consumption. The buffer layers also exhibit higher resistivity, which should reduce excess gate leakage current and improve device isolation.

Key words: InAs, AlGaSb, high-electron-mobility transistor (HEMT), molecular beam epitaxy (MBE), field-effect transistor (FET), buffer layer

INTRODUCTION

High-electron-mobility transistors (HEMTs) with InAs channels and antimonide barriers were first reported over 20 years ago.[1–3] Advantages of this material system, as discussed in a recent review,[4] include the high electron mobility (30,000 cm^2/V s at 300 K) and velocity (4×10^7 cm/s) of InAs, and the large conduction-band offset between InAs and AlGaSb (>1 eV). The large offset results in good carrier confinement and enhanced radiation tolerance.[5] Advances included a unity current–gain cutoff frequency, f_T, of 250 GHz for a 100 nm gate length at a drain–source bias of 0.6 V,[6] and a demonstration of the potential for extremely low-power consumption with f_T of 90 GHz at a bias of only 100 mV.[7]

In recent years, a variety of monolithic microwave integrated circuits (MMICs) have been demonstrated utilizing InAs HEMT technology. Low-noise amplifier (LNA) MMICs were reported by teams led by Northrop–Grumman and Teledyne Corporations. The LNAs operate in the X-band,[8] Ka-band,[9] and W-band.[10,11] For example, a three-stage W-band LNA was demonstrated with 11 dB gain at a total chip dissipation of only 1.8 mW at 94 GHz. This is a factor of 30 lower power than comparable GaAs-based LNAs at the same frequency.[10] In addition, low-power wideband LNAs have been demonstrated.[12]

InAs and the (In,Ga,Al)Sb alloys have lattice constants greater than 0.6 nm. Unfortunately, there are no suitable zincblende insulating substrates with these lattice constants. As a result, semi-insulating GaAs or InP substrates are used, with strain-relaxed buffer layers to accommodate the 4% to 15% lattice mismatch. AlSb or alloys of AlGaSb have usually been used as buffer layers. Nguyen et al. achieved InAs quantum wells with low-temperature mobilities exceeding 600,000 cm^2/V s, using buffer layers that were 2 μm to 3 μm thick.[13] As a result of such demonstrations, nearly all designs of InAs HEMTs incorporated 1.5-μm- to 3.0-μm-thick metamorphic buffer layers. Such thick layers were suitable for discrete devices but are problematic in the fabrication of MMIC circuits, with associated large-scale manufacturing costs.

One obvious disadvantage of thick buffer layers is growth time. At typical growth rates near 1.0 μm/h, a 2-μm buffer layer will require 2 h of growth time, compared with only a few minutes for the active region of the HEMT. Another disadvantage is

(Received April 7, 2010; accepted May 12, 2010; published online June 12, 2010)

depletion of the group III sources (Al and Ga) as well as the Sb source. In addition, some of the flux from an Sb cell in a molecular beam epitaxy (MBE) system will deposit near the mouth of the cell, eventually causing partial blockage of the Sb beam. Another important issue is buffer layer conductivity. In some cases, conduction through the AlGaSb buffer layer can be the source of a detrimental gate leakage current and can also preclude good isolation between devices. A thinner buffer layer should be less conductive.

In addition to the work on *n*-channel HEMTs described above, there have been recent efforts to achieve low-power, antimonide-based, *p*-channel field-effect transistors (FETs). Ultimately, these could be combined with HEMTs in complementary circuits for digital or mixed-signal applications. Buffer layers of 1 μm to 3 μm have been used in the GaSb/AlAsSb,[14] InSb/InAlSb,[15] and InGaSb/AlGaSb[16,17] materials systems. The use of strain has enhanced hole mobilities to 800 $cm^2/V\,s$ to 1500 $cm^2/V\,s$ at room temperature.

In this work, we investigate AlGaSb buffer layers that are thinner, and grown faster, than antimonide buffer layers used in the past for transistors. We show that smooth surfaces and high carrier mobilities can be achieved. In addition, the thinner buffer layers exhibit substantially higher resistivity.

EXPERIMENTAL PROCEDURES

A typical HEMT heterostructure is shown in Fig. 1a. Growths were performed by solid-source MBE in a Riber 21T system. The oxide was removed from the semi-insulating GaAs (100) substrate by heating the sample to 630°C under As_2 flux. A 30-period (8 nm AlAs/2 nm GaAs) superlattice was then grown at 600°C. After growth of the superlattice, the substrate temperature was lowered to 530°C for growth of an $Al_{0.8}Ga_{0.2}Sb$ buffer layer to accommodate the 8% lattice mismatch. AlGaSb was chosen because it is much less reactive than pure AlSb.[18] The substrate temperature was then lowered to 500°C for growth of an additional 100 nm of $Al_{0.8}Ga_{0.2}Sb$. This was followed by a 12 nm InAs channel. The temperature was then reduced to 450°C for the remaining layers: a 5 nm $In_{0.2}Al_{0.8}Sb$ spacer, a 5 nm Te-doped $In_{0.2}Al_{0.8}Sb$ layer,[19] a 3 nm undoped $In_{0.2}Al_{0.8}Sb$ layer, and a 2 nm undoped InAs cap. The growth rate was 1.0 monolayers (ML)/s for the $In_{0.2}Al_{0.8}Sb$ and 0.4 ML/s for the InAs. It was intentionally varied for the AlAs/GaAs superlattice and $Al_{0.8}Ga_{0.2}Sb$ buffer layer. Migration-enhanced epitaxy was used at the interfaces between InAs and AlGaSb or InAlSb to achieve InSb-like bonds.[20,21] The growth process was similar to that used for InAs-channel transistor structures in the past; more details are given elsewhere.[22,23] The band diagram for our heterostructures, calculated using the Nextnano program,[24] is shown in Fig. 1b. Note the large conduction-band offset,

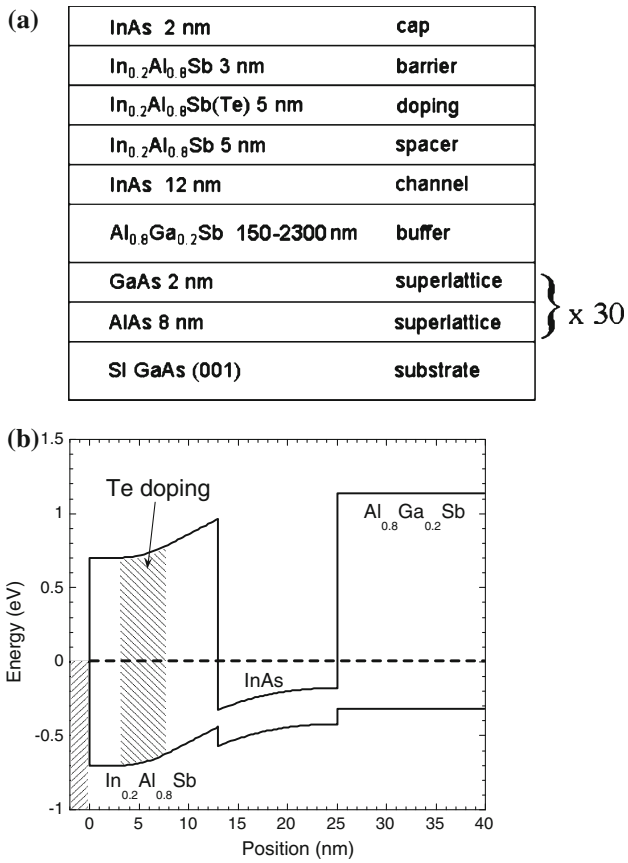

Fig. 1. Cross-section (a) and calculated band structure (b) of InAs quantum well heterostructures. The GaAs/AlAs superlattice is included for calibration.

allowing confinement of electrons in the InAs channel.

Based upon previous results on this MBE system, we expect the layer thicknesses to be uniform to within 1% across the 76-mm-diameter substrate if the wafer is rotated. The wafers were rotated during the InAlSb and InAs layer growths. They were not rotated during the growth of the AlAs/GaAs superlattice or $Al_{0.8}Ga_{0.2}Sb$ buffer layer, resulting in substantial variations in growth rates and layer thicknesses. The purpose of the superlattice is to allow x-ray calibration of the AlAs and GaAs rates, and hence the AlGaSb growth rate and buffer layer thickness.

Several 5 mm × 5 mm squares were cleaved from each 76-mm wafer. Because of the large variations in buffer layer growth rate and thickness, each of these squares constitutes a separate sample. Hall/van der Pauw transport measurements were performed on a total of 53 such 5 mm × 5 mm samples at 300 K and 77 K, using magnetic fields of 0.37 T and 0.55 T. Measurements were performed at two or more currents at each *B*-field. Room-temperature, 55-point resistivity maps were generated for each wafer from eddy-current measurements using a contactless Lehighton 1500 system.[25] Atomic force microscopy

(AFM) measurements were performed on selected samples to yield root-mean-square (rms) roughness over 5 μm × 5 μm regions. X-ray diffraction (XRD) measurements were made on a double-crystal system using Cu K_α radiation and compared with simulations using dynamical diffraction theory.

Additional samples were grown to investigate buffer layer resistivity. These samples were rotated throughout the entire growths. Most were single layers of $Al_xGa_{1-x}Sb$ on semi-insulating GaAs. In some cases, heterostructures including HEMT layers were used, and the HEMT layers were removed by wet chemical etching, allowing transport measurements of the buffer layers. For the most resistive buffer layers, conventional Hall-effect transport measurements were not possible due to the high resistivity of the material. Rectangular pieces (~10 mm × 1 mm) of the material were scribed, and InSn metal contacts were soldered along the opposite edges of the sample. The resistance of the epitaxial material was then determined from direct voltage–current measurements, and the sheet resistivity was calculated, assuming that the resistivity of the semi-insulating substrate was much greater than that of the epitaxial layer. For samples on which Hall-effect measurements were possible, the two techniques yielded resistivities that were within a factor of two.

RESULTS AND DISCUSSION

A total of eight HEMT structures were grown, with large variations in the AlGaSb buffer layer growth rate and thickness across each sample. The only nominal differences in the eight growths were the Ga and Al fluxes and the buffer layer growth times. Figure 2 shows a Lehighton resistivity map for growth 3. The resistivity values are given in units of Ω/□. Thirteen 5 mm × 5 mm samples were cleaved, and are indicated by the letters A–M. The samples from this growth are referred to as 3A, 3B, 3C, etc. The highest growth rates were on the right side of the sample. The cloudy region resulted from an anion (Sb) flux that was less than the cation (Ga + Al) flux. The rms roughness is indicated for three of the samples, and ranged from 0.4 nm to 0.7 nm. Resistivity values calculated from room-temperature Hall measurements ranged from 290 Ω/□ to 370 Ω/□ for samples 3A, 3C, 3E, 3G, 3H, and 3J, in reasonable agreement with the Lehighton values.

The upper trace of Fig. 3 is an x-ray scan from sample 3J. A series of superlattice satellite peaks are present on either side of the GaAs substrate peak. The thicknesses of the AlAs and GaAs layers were adjusted to yield a simulation (lower trace) with satellite peaks in the same positions as the experimental data. In this case, the result was: 9.20 nm AlAs and 2.00 nm GaAs. From these values and the growth times, the growth rates of AlAs and GaAs were calculated to be 1.098 ML/s and 0.241 ML/s, respectively. The same Ga and Al cell

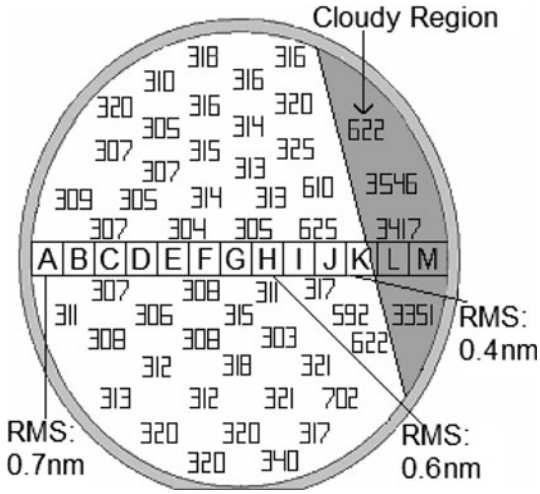

Fig. 2. Resistivity map of growth 3 in units of Ω/□. Thirteen 5 mm × 5 mm squares were cleaved and are labeled as samples 3A–3M. The substrate was not rotated during growth of the buffer layers, resulting in an AlGaSb growth rate which increased from left to right. The shaded portion on the right side represents a cloudy region with insufficient Sb flux. Surface roughness measured by AFM is indicated for three samples.

temperatures were used for the superlattice and the AlGaSb buffer layer. Hence, the growth rate of the AlSb was $1.098 \times (a_{AlSb}/a_{AlAs})^2 = 1.098 \times (6.1355/5.661)^2 = 1.290$ ML/s; similarly, for GaSb: $0.241 \times (a_{GaSb}/a_{GaAs})^2 = 0.241 \times (6.0954/5.6533)^2 = 0.281$ ML/s. Hence, the growth rate for the AlGaSb buffer layer is 1.57 ML/s. The growth time was 2560 s, yielding a buffer layer thickness of 1.23 μm. The peak corresponding to the AlGaSb buffer layer is at −10,300 arcsecond in Fig. 3. Peaks are also visible for the 12 nm InAs channel and the 13 nm InAlSb barrier layers. The full-width at half-maximum (FWHM) of the AlGaSb layer is 370 arcsecond, compared with 16 arcsecond for the simulation. This broadening is the result of a high density of misfit dislocations that relieve the 8% lattice mismatch. Figure 4 shows a plot of AlGaSb FWHM as a function of layer thickness for the 23 samples in the study measured by XRD. The FWHM values range from 620 arcsecond for a 0.15 μm layer to 290 arcsecond for a 2.3 μm layer; simulated values for dislocation-free films are 110 arcsecond and 11 arcsecond, respectively. Narrower peak widths are generally considered to reflect better crystalline quality. The trend here is consistent with the expectation that the dislocation density will decrease when moving away from the interface.

Figure 5 illustrates the dependence of room-temperature mobility on AlGaSb buffer layer growth rate and thickness. Each of the squares indicates a 5 mm × 5 mm sample for which the growth rate and thickness were calculated from x-ray measurements, as described above. The circles represent samples for which the growth rate and thickness were interpolated from the x-ray results on adjacent

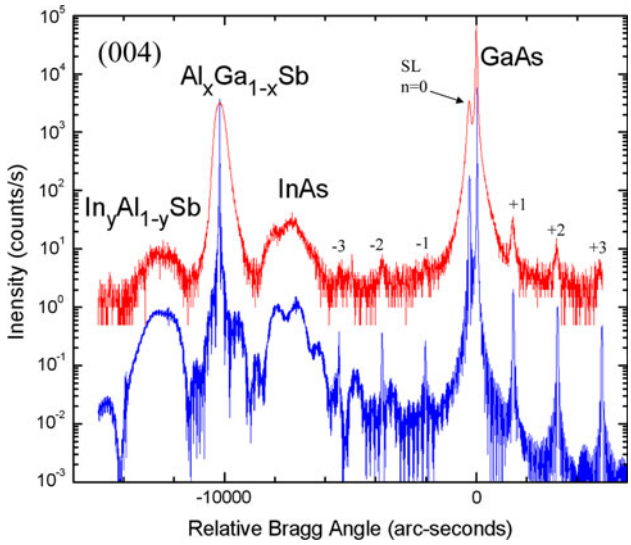

Fig. 3. Double-crystal XRD scan for sample 3J (*upper trace*) and simulation (*lower trace*). The growth rate and layer thickness of the AlGaSb buffer were calibrated by using the AlAs/GaAs superlattice satellite peaks.

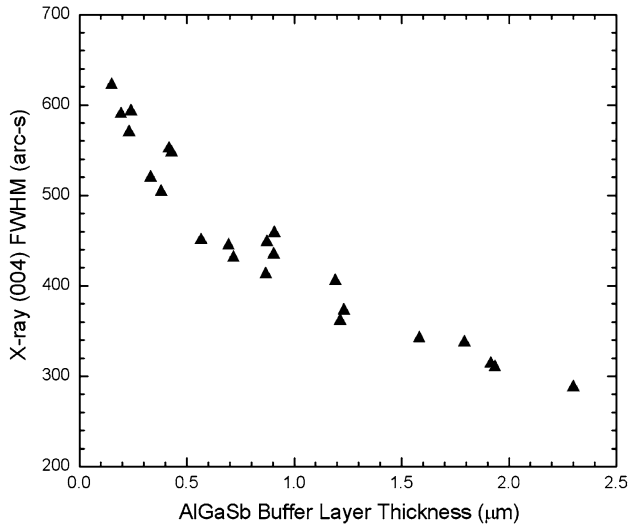

Fig. 4. AlGaSb buffer layer (004) x-ray FWHM as a function of layer thickness.

samples in the same growth. For example, samples 2I and 2J were interpolated from 2H and 2K. The number next to each data point represents the measured room-temperature mobility ($\times 10^3$ cm^2/V s) of the InAs quantum well. For each sample, at least four measurements were averaged.

The cross-hatched region in Fig. 5 indicates the buffer layer parameters usually used by our group and others in the past.[4,26] A notable exception was the work by Kuze et al.[27] which demonstrated high electron mobility in InAs quantum wells on 0.6 μm AlGaAsSb buffer layers. There were also previous reports of high-mobility InAs quantum wells on AlSb buffers grown at 2.0 ML/s.[28,29] We see that high mobilities can be achieved for buffer layers that are thinner and grown faster than normal. For example, sample 5M, with a buffer thickness of 0.57 μm and growth rate of 1.13 ML/s, had a room-temperature mobility of 23,800 $\pm$ 2200 cm^2/V s. Sample 6J, with a buffer thickness of 0.90 μm and a growth rate of 1.91 ML/s, had a room-temperature mobility of 22,400 $\pm$ 800 cm^2/V s. All of our samples with a buffer layer thickness greater than 0.5 μm had mobilities greater than 20,000 cm^2/V s. Sheet carrier densities varied between 0.7×10^{12}/cm^2 and 1.2×10^{12}/cm^2 with no clear correlation to buffer layer thickness or growth rate. Within a single growth, the variations were smaller, e.g., 1.05×10^{12}/cm^2 to 1.14×10^{12}/cm^2 for growth 1.

In Fig. 6, we plot room-temperature mobility versus buffer layer thickness and include all samples with growth rates between 1.40 ML/s and 1.60 ML/s. Degradation in mobility is observed for thinner buffer layers, with values near 18,000 cm^2/V s and 14,000 cm^2/V s for thicknesses near 0.4 μm and 0.2 μm, respectively. We note that our group and others have reported room-temperature electron mobilities in the 25,000 cm^2/V s to 30,000 cm^2/V s range for InAs quantum wells. It is not always clear why these higher values are sometimes achieved, but careful optimization of the arsenic flux may be important in some cases.[27,30,31] In this work, we did not attempt to optimize the arsenic flux. For growths 1 through 6, the 77-K mobilities ranged from 44,000 cm^2/V s to 79,000 cm^2/V s with no obvious correlation with buffer layer thickness or growth rate. The 77-K mobilities dropped to 30,000 cm^2/V s and 25,000 cm^2/V s, respectively, for growths 7 and 8, consistent with the lower room-temperature mobilities.

Selected samples, including at least one from each growth, were measured by AFM. In Fig. 7, we show a 5 μm $\times$ 5 μm scan of sample 5H. This sample had a 0.69 μm buffer layer grown at 1.38 ML/s. The rms roughness was 0.6 nm, and the peak-to-valley height was 5 nm. For the other samples, the rms roughness ranged from 0.3 nm to 1.4 nm. This entire range of values is very good. This result shows that relatively large x-ray FWHM values (e.g., 620 arcsecond for a 150 nm layer) do not preclude smooth surfaces for these heterostructures. In previous work on InAs-channel HEMTs [with Al(Ga)Sb buffer thicknesses of 2.0 μm to 2.4 μm] we found that rms values of 0.5 nm to 3.5 nm were consistent with high mobilities and MMIC fabrication processes.[22,30] The ability to achieve smooth surfaces after relatively thin buffer layers of Al-rich AlGaSb on GaAs is consistent with our previous scanning tunneling microscopy images of 100-nm layers of AlSb on GaAs.[32] In our current work, we observed no obvious correlation between rms roughness and electron mobility, buffer layer growth rate, or buffer layer thickness over the ranges investigated. We did, however, observe an apparent correlation between V:III flux ratio and

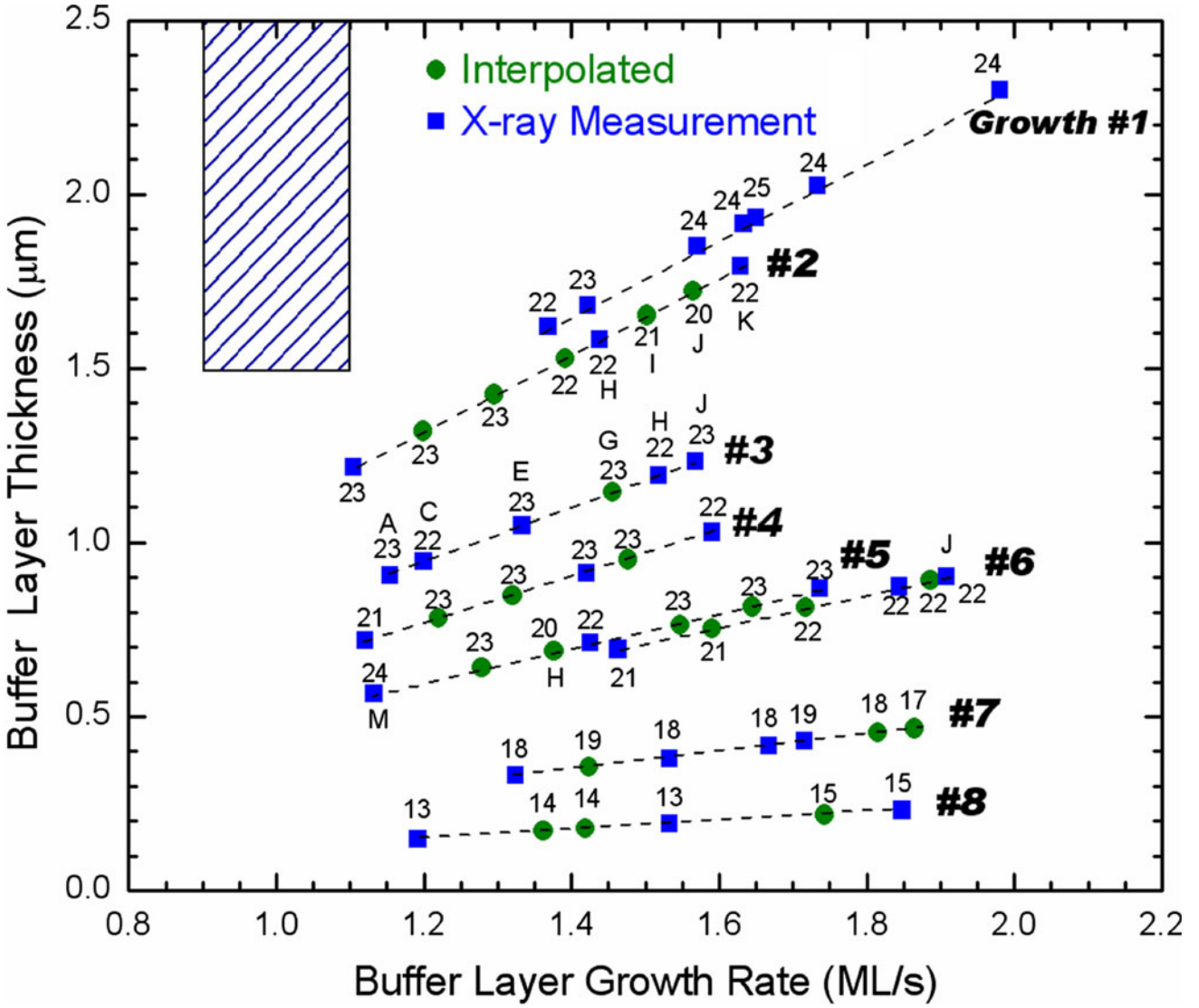

Fig. 5. AlGaSb buffer thickness versus growth rate; the *number* next to each data point is the room-temperature electron mobility ($\times 10^3$ cm^2/V s). Sheet carrier densities ranged from 0.7 $\times$ 10^{12}/cm^2 to 1.2 $\times$ 10^{12}/cm^2. Samples discussed in the text are identified by *letter*. The *shaded region* represents the parameters used in most previous work.

rms roughness. For example, in growth 3 (Fig. 2), the rms roughness is smallest (0.4 nm) for sample 3K, which borders on the cloudy, anion-deficient region. This sample should have a V:III flux ratio near 1.0:1. Samples 3H and 3A have higher V:III ratios and exhibit rougher surfaces, with rms roughness of 0.6 nm to 0.7 nm. We observed similar trends on other samples. One possibility is that the higher flux ratios reduce the cation mobilities, resulting in rougher surfaces.[33] We emphasize that all the samples exhibited relatively smooth surfaces.

Our rough estimate is that V:III ratios are 2:1 near the wafer edge with the lowest group III fluxes, e.g., sample 3A on Fig. 2. High mobilities and smooth surfaces are achieved for ratios between 2:1 and 1:1. In a situation in which the Sb flux is not carefully monitored and adjusted, or is not uniform across the substrate, a target of 1.5:1 might be sensible to avoid the possibility of being anion deficient. On the other hand, in a production environment with careful monitoring of Sb flux, a target of 1.1:1 would minimize Sb use and flux blockages resulting from Sb build-up around the cell port.

As discussed earlier, previous work on *p*-channel, Sb-based FETs used buffer layers at least 1.0 μm thick. Based upon our HEMT results, we grew a 7.5 nm quantum well of $In_{0.4}Ga_{0.6}Sb$ on a 0.6 μm $Al_{0.8}Ga_{0.2}Sb$ buffer grown at 1.5 ML/s. The room-temperature hole mobility was 810 cm^2/V s at a density of 1.1 $\times$ 10^{12}/cm^2, suggesting that these thinner, faster buffer layers may also be suitable for *p*-FET structures.

Previous work on InAs-channel HEMTs often included buffer layers of pure AlSb. They exhibited high resistivity ($\sim$100 M$\Omega/\square$), resulting in good isolation between devices.[34] Because of the high

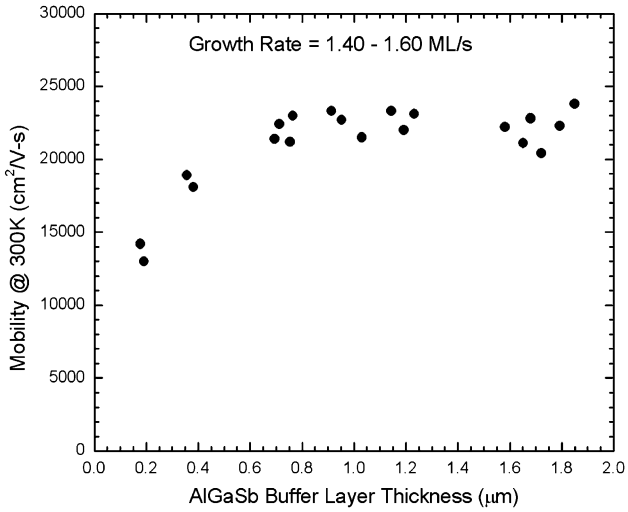

Fig. 6. Room-temperature electron mobility versus AlGaSb buffer thickness for growth rates of 1.5 ± 0.1 ML/s.

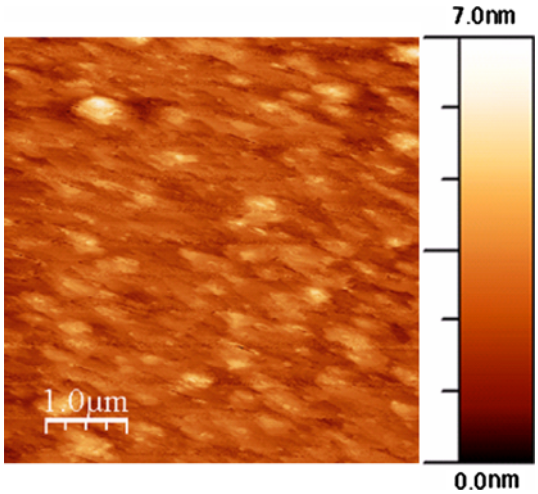

Fig. 7. AFM image of sample 5H with a 0.69 μm buffer layer grown at 1.38 ML/s. The rms roughness was 0.6 nm.

reactivity of AlSb, AlGaSb is often used in its place. Unfortunately, the resistivity is much lower. For example, one group recently reported $Al_{0.7}Ga_{0.3}Sb$ with a resistivity of only 0.01 MΩ/□.[35] To investigate buffer layer resistivity, we grew three 1.5 μm layers of $Al_{0.7}Ga_{0.3}Sb$, varying only the growth temperature. The results are shown in Table I. Samples Buff1 and Buff2, grown at 430°C and 510°C, respectively, had resistivities of 0.7 MΩ/□ to 0.8 MΩ/□. When the growth temperature was increased to 575°C, however, the resistivity dropped to 0.1 MΩ/□. AFM measurements revealed smooth surfaces (rms = 1.2 nm to 1.3 nm) for Buff2 and Buff3, but a somewhat rougher surface (rms = 2.3 nm) for Buff1. Based on these results, a growth temperature of 510°C was selected for additional growths. For Buff4, a digital alloy of AlSb/GaSb was grown, with 490 repeats of (7 ML AlSb/3 ML GaSb)

Table I. Samples for buffer layer resistivity study

Name	Structure	Al (%)	T_{sub} (°C)	t (μm)	R_s (MΩ/□)
Buff1	Single layer	70	430	1.5	0.8
Buff2	Single layer	70	510	1.5	0.7
Buff3	Single layer	70	575	1.5	0.1
Buff4	Digital alloy	70	510	1.5	0.2
Buff5	HEMT	80	510	1.5	10
Buff6	HEMT	80	510	1.5	8
Buff7	Single layer	80	510	1.5	5
Buff8	Single layer	80	510	0.6	77

The AlSb mole fraction in $Al_xGa_{1-x}Sb$, substrate temperature during growth, buffer layer thickness, and resistivity are included.

for an effective composition of $Al_{0.7}Ga_{0.3}Sb$. The hypothesis was that the energy levels of traps relative to the conduction and valence bands would be modified, resulting in a change in resistivity. The resistivity decreased by a factor of four compared with Buff2. Room-temperature hole mobilities for Buff1 through Buff4 were 100 cm^2/V s to 200 cm^2/V s.

The AlSb mole fraction was increased to 80% for four additional samples. Buff5 and Buff6 included HEMT layers which were removed before the resistivity measurements on the remaining 1.5 μm $Al_{0.8}Ga_{0.2}Sb$ layers. Buff7 was a single 1.5 μm $Al_{0.8}Ga_{0.2}Sb$ layer without any HEMT structure. The three samples exhibited resistivities of 5 MΩ/□ to 10 MΩ/□, about an order of magnitude higher than Buff2. It was, in part, this result that led us to select $Al_{0.8}Ga_{0.2}Sb$ for the composition of the buffer layers in HEMT growths 1 to 8 discussed earlier in this paper. The final sample, Buff8, was a single 0.6 μm layer of $Al_{0.8}Ga_{0.2}Sb$ and had a resistivity of 77 MΩ/□. If conductivity were proportional to the layer thickness, we would only expect a factor of 2.5 increase in resistivity compared with Buff5 to Buff7. The larger increase suggests significant band bending, with a depletion region occupying a significant fraction of the buffer layer.[36]

CONCLUSIONS

This work demonstrates that InAs quantum wells can be grown on AlGaSb buffer layers which are thinner, and grown faster, than has been used heretofore. Room-temperature mobilities exceeded 20,000 cm^2/V s for layers as thin as 0.57 μm. Some degradation in mobility occurs for thinner samples, but surfaces remain smooth for layers at least as thin as 0.15 μm. These thinner buffer layers, combined with faster growth rates (1.5 ML/s to 2.0 ML/s), can reduce typical buffer layer growth times from about 2 h to less than 30 min. In addition, the thinner layers result in less conductive buffer layers, which will reduce gate leakage current and improve device isolation in circuits.

ACKNOWLEDGEMENTS

The authors thank Dr. M.G. Ancona for band structure calculations and the Office of Naval Research for support.

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