Antimonide based compound semiconductors have gained considerable interest in recent years due to their superior electron and hole transport properties.\(^1,2\) Mixed anion In\(_{a}Sb_{1−a}\) quantum-well structures (QWs) with high electron mobility are candidates for integration with high hole mobility In\(_{y}Ga_{1−y}\)Sb quantum-well structures (QWs) for low power complementary logic applications.\(^3\) Recently, In\(_{a}As_{1−a}Al_{y}Ga_{1−y}\)Sb heterojunction tunnel field effect transistors (H-TFETs) have been proposed for low-power-high-performance applications.\(^4\) Integrating a high quality dielectric is key to demonstrating a scalable metal-oxide-semiconductor QWFET (MOS-QWFET) or H-TFET architecture for low-power logic applications. We hypothesize that an ultrathin GaSb surface layer is more favorable toward high-\(\kappa\) dielectric integration than Al\(_{y}Ga_{1−y}\)Sb barrier layer for the QWFET or Al\(_{y}Ga_{1−y}\)Sb channel layer for the H-TFET, as it avoids Al at the interface and the associated surface oxidation. Hence, it is imperative to carefully examine the electrical characteristics of high-\(\kappa\)/GaSb semiconductor interface.

GaSb has a highly reactive surface and on exposure to air it will form a native oxide layer composed of Ga\(_2\)O\(_3\) and Sb\(_2\)O\(_3\) (2GaSb + 3O\(_2\) → Ga\(_2\)O\(_3\) + Sb\(_2\)O\(_3\)). The Sb\(_2\)O\(_3\) can further react with the GaSb surface forming elemental Sb and Ga\(_2\)O\(_3\) (Sb\(_2\)O\(_3\) + 2GaSb → Ga\(_2\)O\(_3\) + 4Sb).\(^5,6\) Chemical treatments based on HCl are effective in removing native oxides on GaSb.\(^6,7\) Here, we study the effects of HCl treatment on the capacitance-voltage characteristics (C-V) and the surface chemistry of n-type and p-type GaSb(100) MOS capacitors fabricated with both atomic-layer-deposited (ALD) and plasma enhanced ALD (PEALD) Al\(_2\)O\(_3\) dielectrics. PEALD was employed to reduce the thermal budget of dielectric deposition, particularly important for antimonide based semiconductors. In this Letter, we demonstrate an unpinned Fermi level in GaSb MOS system with a high-\(\kappa\) PEALD Al\(_2\)O\(_3\) dielectric, using temperature resolved admittance spectroscopy and monochromatic x-ray photoelectron spectroscopy (XPS) analysis.

Both n-type and p-type GaSb (100) MOS capacitors were fabricated with high-\(\kappa\) Al\(_2\)O\(_3\) gate dielectric. The samples were degreased in acetone and ethanol for 5 min each and rinsed in isopropyl alcohol (IPA). The degrease step was followed by a dip in concentrated HCl (HCl:H\(_2\)O = 1:2) for 5 min to remove surface oxides followed by an IPA rinse. GaSb MOS capacitors were fabricated with Al\(_2\)O\(_3\) deposited by ALD at 300 °C from trimethylaluminum (TMA) and water or by PEALD at 200 °C from TMA and CO\(_2\). Pt/Au gate metallization was done using electron beam evaporation after defining gate patterns using optical lithography. Pd/Au backside Ohmic contacts were deposited using electron beam evaporation. No post deposition anneal was done for any of the samples.

Capacitance voltage (C-V) and conductance voltage (G-V) measurements were obtained with HP 4285A precision LCR meter. Figure 1(a) shows the C-V measurements on ALD Al\(_2\)O\(_3\)/n-GaSb and PEALD Al\(_2\)O\(_3\)/n-GaSb MOS capacitors. The ALD sample shows weakly pinned C-V characteristics with very fast interface trap density (D\(_{it}\)) response whereas PEALD sample demonstrates good Fermi level modulation. The accumulation side of C-V characteristics for the PEALD sample shows the effect of high D\(_{it}\) near the conduction band (CB) and the negative bias regime shows the effect of inversion response along with a low D\(_{it}\) response. The accumulation side of the admittance data is analyzed using the standard depletion/accumulation model\(^8\) and the inversion side using an alternative.\(^9\) The circuit model in inversion accounts for the supply of minority carriers through bulk thermal generation and diffusion across the space charge layer along with interface state contribution, which enables accurate modeling of the admittance data in inversion. Figure 1(b) shows C-V characteristics of the ALD Al\(_2\)O\(_3\)/p-GaSb and PEALD Al\(_2\)O\(_3\)/p-GaSb samples with HCl treatment for different temperatures. The ALD sample shows strongly pinned C-V characteristics with both accumulation and inversion regimes completely dominated by interface states. For the PEALD sample, there is minimal dispersion of capacitance in accumulation due to less D\(_{it}\) near
the valence band (VB) whereas the inversion response shows contributions from minority carriers as well as high Dit near the CB. The 200 K C-V shows a clear Fermi level movement from accumulation to depletion for the PEALD sample whereas ALD sample exhibits pinned C-V characteristics. C-V measurements for the n-type and p-type MOS capacitors were done at 300 and 250 K (300 and 200 K). The reason is that the backside contact (Pd/Au) on GaSb is Ohmic for holes whereas it forms a Schottky barrier for electrons (~0.6 eV Schottky barrier height for electrons due to the Fermi stabilization energy in GaSb being ~0.1 eV from the VB. This Schottky barrier gives rise to higher contact resistance for electrons at lower temperatures, which causes frequency dispersion in the accumulation capacitance of the n-type metal-oxide-semiconductor capacitors (MOSCAPs). For the p-type devices this is not a problem as the contacts are Ohmic for holes, and the measurement can be done at very low temperature. Hence, the above measurement temperatures were employed.

Figure 2 shows the conductance contour map (G/ω) of n-type and p-type PEALD samples as a function of gate voltage and small-signal frequency. The V-shaped trajectory of the peak value of conductance, (G/ω) peak, along the frequency axis shows that the Fermi level moves freely on either side of the midgap of GaSb. PEALD Al₂O₃/GaSb samples demonstrate an unpinned Fermi level at the interface, even though the Fermi stabilization energy for GaSb is 0.1 eV from the VB. The extracted capture cross section values are 9 × 10⁻¹⁵ cm² for traps near the VB and 8 × 10⁻¹⁹ cm² for traps near the CB, indicating that the traps near the VB are faster than those near the CB. Hence, the conductance plots were done at lower temperature for the p-type samples where the conductance peaks were visible. The capture cross section values are consistent with Ref. 12, where irradiated p-type GaSb showed acceptor type traps near the VB with higher capture cross-section.

Figure 3 shows the monochromatic XPS analysis of the Sb 4d region for the ALD and PEALD samples with HCl treatment. All PEALD and ALD samples show presence of Ga-oxides. The ALD samples show no detectable Sb-oxides whereas the PEALD samples have significant Sb-oxides. As
In summary, we have demonstrated GaSb MOS capacitors (p-type and n-type) with unpinned Fermi level using PEALD Al2O3 by minimizing elemental Sb at the GaSb/Al2O3 interface. The reduction of Sb2O3 to metallic Sb is suppressed with PEALD due to lower deposition temperature, which is confirmed by XPS analysis. The Dv is low near the valence band which makes GaSb-PEALD Al2O3 a good interface for composite barrier design with AlxIn1-xSb and AlxGa1-xSb barrier layers in mixed-anion MOS-QWFETs or H-TFETs for ultralow power logic applications.

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13Details of the XPS analysis system are described in: R. M. Wallace, ECS Trans. 16(5), 255 (2008).