Advanced Composite High-κ Gate Stack for Mixed Anion Arsenide-Antimonide Quantum Well Transistors

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Abstract
This paper demonstrates the integration of a composite high-κ gate stack (3.3 nm Al₂O₃-1.0 nm GaSb) with a mixed anion InAs₀.₈Sb₀.₂ quantum-well field effect transistor (QWFET). The composite gate stack achieves; (i) EOT of 4.2 nm with <10⁻¹²/A/cm² gate leakage (ii) low Dᵥ interface (~1x10¹²/cm²/eV) (iii) high drift µ of 3,900–5,060 cm²/V·s at N_s of 5x10¹¹–3x10¹²/cm². The InAs₀.₈Sb₀.₂ MOS-QWFETs, where the surface Fermi level suppressions (Figs. 4a,b). Figs. 3 shows the schematic of the InAs₀.₈Sb₀.₂ MOS QWFET with GaSb and Al₂O₃ dielectric which forms a composite gate stack on top of the QW. Figs. 5 shows the energy band diagram of the InAs₀.₈Sb₀.₂ QW structure with the composite Al₂O₃-GaSb gate stack using Schrodinger-Poisson simulation, indicating strong electron confinement in the InAs₀.₈Sb₀.₂ QW.

Introduction
Mixed anion InAs₀.₈Sb₀.₂, quantum-wells (QW) with high electron mobility are candidates for integration with high hole mobility In₀.₇Ga₀.₃ As QW for ultra-low power complementary applications. With the exception of a recent In₀.₇Ga₀.₃As QWFET with high-κ gate stack, nearly all QWFETs, reported to date, use Schottky gates and suffer from high gate leakage. For further scaling, a gate stack is needed for integration with InAs₀.₈Sb₀.₂ QWFET, with low EOT and J₀X, good interface properties and high carrier mobility in the channel. Here, we integrate a composite high-κ gate stack (Al₂O₃-GaSb) with InAs₀.₈Sb₀.₂ QWFET, resulting in high performance transistors operating at 0.5V V_DS.

Materials Characterization
MBE grown mixed anion InAs₀.₈Sb₀.₂ QW exhibit room temperature electron mobility between 11,000–22,000 cm²/V·s with varying electron density, corresponding to ballistic mean free path of ~400nm, making them promising channel material candidates for high-speed, low power electronics (Fig. 1). To retain the high carrier mobility in InAs₀.₈Sb₀.₂ QWFET, the high-κ dielectric is deposited on the upper barrier and not directly on the channel. We incorporated an ultra-thin (1nm) GaSb layer in the upper barrier as it avoids Al at the interface and associated surface oxidation. Using n-type and p-type GaSb(100) MOS capacitors, we evaluated both ALD and Plasma Enhanced ALD (PEALD) Al₂O₃ dielectrics and confirmed unpinned Fermi level in GaSb MOS system with the latter (Fig. 2a). By minimizing elemental Sb at the GaSb/Al₂O₃ interface using the low temperature PEALD Al₂O₃, we demonstrate low Dᵥ (~1x10¹² /cm²/eV) near the valence band making the composite 3.3nm Al₂O₃/1nm GaSb gate stack suitable for InAs₀.₈Sb₀.₂ QWFETs, where the surface Fermi level sweeps below the midgap of GaSb towards the valence band (Fig. 2b). From XPS measurements we estimate the valence and conduction band offsets to be 3.4eV and 2.4eV respectively, sufficient for gate leakage suppression (Figs. 4a,b). Figs. 3 shows the schematic of the InAs₀.₈Sb₀.₂ MOS QWFET with GaSb and Al₂O₃ dielectric which forms a composite gate stack on top of the QW. Figs. 5 shows the energy band diagram of the InAs₀.₈Sb₀.₂ QW structure with the composite Al₂O₃-GaSb gate stack using Schrodinger-Poisson simulation, indicating strong electron confinement in the InAs₀.₈Sb₀.₂ QW.

Device Characterization
Figs. 9a,b show the top view SEM and cross-section TEM of the InAs₀.₈Sb₀.₂ MOS QWFET with 100nm physical gate length (L_G) and the composite Al₂O₃-GaSb gate stack. Pd/Pt/Au metal stack was alloyed to form embedded contacts making direct contact with the QW (Fig.10). Circular TLM measurements before and after PEALD Al₂O₃ deposition are shown in Fig. 11. Figs. 12a,b show the split C-V_G characteristics of InAs₀.₈Sb₀.₂ MOS-QWFET for 4.4nm and 3.3nm physically thick Al₂O₃ and the frequency dispersion characteristics. The EOT of the thinner stack is 4.2 nm which includes the 9 nm Al₂O₃/In₀.₂Sb barrier and 12 nm InAs₀.₈Sb₀.₂ QW capacitance. Conductance vs frequency contour plot (Figs. 13a,b) shows positive slope with V_G indicating electron capture/emission process. This could be due to...
the traps at the oxide-GaSb interface. Fig. 14 plots $J_{OX}$ vs $V_G$ showing less than $10^{-7}$ A/cm$^2$ of gate leakage in InAs$_{0.8}$Sb$_{0.2}$ MOS-QWFET. Room temperature drift mobility values of 3,900-5,060 cm$^2$/V-s at carrier concentrations of $5 \times 10^{11}$-$3 \times 10^{12}$/cm$^2$ are extracted from split C-V data (Fig. 15). Figs. 16-17 show the drain current ($I_D$) vs. gate voltage ($V_G$) of InAs$_{0.8}$Sb$_{0.2}$ MOS-QWFET for various $L_G$ and $L_{SIDE}$. Parasitic access resistance limits the achievable on-current in the fabricated devices. For the shortest $L_{SIDE}$ of 0.25µm and $L_G = 1$µm, the best extrinsic $g_m$ and $I_D$ at 300K are 334 µS/µm and 380 µA/µm, and at 77K are 630 µS/µm and 411 µA/µm at $V_{DS} = 0.5$V. Peak intrinsic gm increases to 502 µS/µm (1,070µS/µm) at 300K (77K) (Fig. 19). Fig. 18 shows the output characteristics of the device at 300K and 77K for $L_G = 1$µm and $L_{SIDE} = 0.25$ µm. The high off-state leakage of InAs$_{0.8}$Sb$_{0.2}$ MOS-QWFET at 300K is likely due to the hole accumulation in the Al$_{0.8}$In$_{0.2}$Sb barrier layer screening the gate potential as well as the generation of holes due to impact ionization. The source side effective injection velocity, $V_{eff}$, is extracted as a function of $V_{GS}$ - $V_T$ at 77K for InAs$_{0.8}$Sb$_{0.2}$ MOS-QWFET (Fig. 20). The highest $V_{eff}$ obtained is 1.4x10$^7$ cm/s, one of the highest values ever reported for III-V MOS QWFETs.

Conclusions

An advanced composite high-$\kappa$ gate stack (3.3nm Al$_2$O$_3$-1.0nm GaSb) is successfully integrated in the mixed anion InAs$_{0.8}$Sb$_{0.2}$ QWFET with low EOT (4.2nm), negligible $J_{OX}$ ($10^{-7}$ A/cm$^2$) and high drift $\mu$ (3,900-5,060 cm$^2$/V-s). The InAs$_{0.8}$Sb$_{0.2}$ MOS-QWFETs with $L_g = 1$ µm exhibit intrinsic transconductance of 502 µS/µm and 1,070 µS/µm and drive currents of 380 µA/µm and 411 µA/µm at room temperature and 77K, respectively, all at $V_{DS} = 0.5$V.

References


Acknowledgement

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Table 1 Percentage contribution to $1/\mu$ at 300K

<table>
<thead>
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<th>Component</th>
<th>Contribution</th>
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<tr>
<td>Interface Charge</td>
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<tr>
<td>ADP Scattering</td>
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<tr>
<td>Remote Ionized Impurity Scattering</td>
<td>13%</td>
</tr>
<tr>
<td>Alloy Scattering</td>
<td>8%</td>
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<tr>
<td>Polar Optical Phonon Scattering</td>
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Fig. 6 (b) High resolution TEM micrograph of InAs$_{0.8}$Sb$_{0.2}$ QW stack with as deposited 2.5nm GaSb (surface preparation prior to oxide deposition reduces GaSb thickness to 1nm)

Fig. 7 (a) Carrier density ($N_s$), and (b) Hall mobility vs temperature for InAs$_{0.8}$Sb$_{0.2}$ QW

Fig. 9 (a) Top view SEM of InAs$_{0.8}$Sb$_{0.2}$ QWFET with composite Al$_2$O$_3$-GaSb gate stack on top of the QW

Fig. 8 (a) Shubnikov-de Haas (SdH) oscillations in the sheet resistance. Temperature dependence of the amplitude of these oscillations is used to calculate $m^*$ (b) FFT of SdH oscillations vs. $1/B$ at 2K (inset) shows single peak confirming majority carrier transport in the first subband of the QW at $n_s=2\times10^{12}$/cm$^2$ and no parallel conduction

Fig. 10 (a) Cross-section TEM of InAs$_{0.8}$Sb$_{0.2}$ MOS QWFET under the alloyed embedded contact directly contacting the InAs$_{0.8}$Sb$_{0.2}$ channel (b) Schematic cross-section of the region underneath the ohmic contact (c) Band diagram explaining the embedded ohmic contact formation

Fig. 11 Circular TLM measurements before and after PEALD Al$_2$O$_3$ deposition
Tox = 4.4 nm
Tox = 3.3 nm

Split Capacitance [μF/cm²]

Gate Voltage [V]

Frequency = 2MHz

T = 77K

T = 77K

T = 4.4 nm

T = 3.3 nm

75KHz to 2MHz

T = 77K

T = 4.4 nm

T = 3.3 nm

Log (Frequency [Hz])

Gate Leakage [A/cm²]

Gate Voltage [V]

77K

300K

4.4nm Oxide

3.3nm Oxide

Gate Leakage [A/cm²]

Gate Voltage [V]

4.4nm Oxide

3.3nm Oxide

Gate Leakage [A/cm²]

Gate Voltage [V]

Gate Leakage [A/cm²]

Gate Voltage [V]

InAs0.8Sb0.2 MOS QWFET with composite stack; peak conductance trace reflects Fermi level movement in the InAs0.8Sb0.2 QW

Fig. 12 (a) Measured split C-VG characteristics of InAs0.8Sb0.2 MOS QWFET with various composite gate stack thickness (b) Frequency dispersion of the C-VG characteristics of InAs0.8Sb0.2 MOS QWFET

Fig. 13 (a-b) G-VG characteristics of InAs0.8Sb0.2 MOS QWFET with 1.0 µm, 500nm, 100nm and Al2O3-GaSb composite stack (EOT= 4.2nm) at 300K and 77K at VDS = 0.5V, 50mV (Lside = 0.5 µm)

Fig. 14 LX vs VG showing lower than 10⁻⁷ A/cm² of gate leakage in InAs0.8Sb0.2 MOS-QWFET

Fig. 15 Drift μ vs N, at 77K and 300K in InAs0.8Sb0.2 MOS QWFET from split C-VG measurements

Fig. 16 LG scaling: Drain current (I_D) vs. gate voltage (V_G) of InAs0.8Sb0.2 MOS-QWFET with LG = 1 µm, 500nm, 100nm and Al2O3-GaSb composite stack (EOT= 4.2nm) at 300K and 77K at VDS = 0.5V, 50mV (Lside = 0.5 µm)

Fig. 17 LSIDE scaling: I_D vs. V_G of LG= 100nm InAs0.8Sb0.2 MOS-QWFET with composite stack at 77K at VDS = 0.5Vwith Lside = 0.5, 1 and 2 µm

Fig. 18 Output Characteristics: I_D vs. V_DS of InAs0.8Sb0.2 MOS-QWFET with LG= 1 µm, Lside = 0.25 µm and Al2O3-GaSb composite stack (EOT= 4.2nm) at 300K and 77K

Fig. 19 Transconductance (g_m) characteristics of InAs0.8Sb0.2 MOS-QWFET with LG= 1 µm, Lside = 0.25 µm and Al2O3-GaSb composite stack (EOT= 4.2nm) at 300K and 77K. Intrinsic peak gm is 502 µS/µm and 1070 µS/µm at 300K and 77K, respectively

Fig. 20 Extracted effective injection velocity, V_eff, as a function of V_GSi-V_T using the charge obtained from split C-VG measurements and I_D,SAT vs V_GSi-V_T. The V_T from split C-VG is matched to the V_T,SAT from I_D,SAT vs V_GSi-V_T to obtain V_eff