$In_xGa_{1-x}Sb$ channel p-metal-oxide-semiconductor field effect transistors: Effect of strain and heterostructure design

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$In_xGa_{1-x}Sb$ is an attractive candidate for high performance III-V p-metal-oxide-semiconductor field effect transistors (pMOSFETs) due to its high bulk hole mobility that can be further enhanced with the use of strain. We fabricate and study $In_xGa_{1-x}Sb$-channel pMOSFETs with atomic layer deposition Al_2O_3 dielectric and self-aligned source/drain formed by ion implantation. The effects of strain and heterostructure design for enhancing transistor performance are studied systematically. Different amounts of biaxial compression are introduced during MBE growth, and the effect of uniaxial strain is studied using wafer-bending experiments. Both surface and buried channel MOSFET designs are investigated. Buried (surface) channel $In_xGa_{1-x}Sb$ pMOSFETs with peak hole mobility of 910 (620) cm^2/Vs and subthreshold swing of 120 mV/decade are demonstrated. Pulsed I-V measurements and low-temperature I-V measurements are used to investigate the physics in transistor characteristics. © *2011 American Institute of Physics*.
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I. INTRODUCTION

III-V semiconductors are considered as promising candidates to selectively replace silicon as the channel material in future technology nodes for transistors, where high performance and low power are required.[1] Most of this research is driven by the excellent electron mobilities in III-V materials. Excellent inversion electron mobility and high on-current (I_{ON}) in n-channel III-V MOSFETs has been demonstrated by many research groups.[2–4] However, the hole mobility achieved in III-V MOSFETs has traditionally lagged in comparison to silicon and has always been lower as compared to germanium pMOSFETs. In this paper, we explore the use of strain engineering and heterostructure design to enhance the hole mobility in III-V channel materials and demonstrate an $In_xGa_{1-x}Sb$ pMOSFET with high hole mobility.

Antimony (Sb)-based compound semiconductors have the highest hole and electron mobilities among all III-V materials. The electron saturation velocity in InSb is the highest among all semiconductor materials. Room-temperature hole mobilities as high as 1500 cm^2/Vs in a strained $In_XGa_{1-X}Sb$ channel at a sheet charge density of around $10^{12}/cm^2$ have also been demonstrated recently.[5] Schottky-gate FET devices with an $In_XGa_{1-X}Sb$ channel have achieved f_T of 305 GHz ($L_G = 85$ nm) for n-channel[6] and f_T of 140 GHz ($L_G = 40$ nm) for p-channel.[7] Thus, $In_XGa_{1-X}Sb$ has the potential to enable a complementary technology with both high performance nMOSFETs and pMOSFETs in a single channel material, outperforming silicon.[8] This approach could be more suitable for integration than one that requires two material systems with different lattice constants for the n-channel and p-channel MOSFETs.[9] In addition to good mobility for the electrons and holes, $In_XGa_{1-X}Sb$ has high conduction and valence band offsets with lattice matched $Al_xIn_{1-x}Sb$ for heterostructure MOSFET design. Lastly, Sb-materials have low melting points, e.g., GaSb has a melting point of 712 °C as compared to 1238 °C for GaAs and 1414 °C for silicon. As the thermal budget for processing scales with melting point, Sb-materials are suitable for low temperature processing, which allows a simpler process flow and can be advantageous when these materials are grown on top of another substrate, e.g., silicon, for heterogeneous integration.

In this paper, we focus on the development and analysis of $In_xGa_{1-x}Sb$ channel pMOSFETs with the aim of achieving a pMOSFET with high hole mobility, which has been an impediment for III-V CMOS. We explore the use of strain and heterostructure design to enhance the transistor performance. Strain has been widely used in the case of silicon pMOSFETs to enhance the hole mobility and transistor performance. In the case of III-V channels, biaxial compressive strain is known to split the light- and heavy-hole bands, reducing the interband scattering and causing the light hole band to move up, increasing hole mobility.[10,11] Simulations have predicted up to 2 times enhancement in hole mobility with the use of 2% biaxial compression.[12,13] Uniaxial strain is predicted to be more effective in enhancing the hole mobility. Modeling results have predicted 4.3 times enhancement in hole mobility with 2% compression along the <110> channel direction.[12] Thus $In_xGa_{1-x}Sb$, with its high bulk hole mobility, which can be further enhanced with the use of strain, is an attractive candidate to deliver a high performance III-V pMOSFET. In the present paper, we incorporate the high mobility $In_xGa_{1-x}Sb$ heterolayers into III-V pMOSFET designs with quality gate dielectric and with a

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self-aligned source/drain technology. The effect of biaxial compression on hole mobility and MOSFET current is studied by engineering the lattice mismatch between the channel and buffer layer. In addition, we investigate the benefits of uniaxial stress using wafer-bending experiments.

The rest of the paper is organized as follows: In Section II, we give the motivation and details on the various transistor designs that were fabricated. Section III gives the details on the MOSFET fabrication. In Section IV, results from the transistors and the effect of strain and heterostructure design are presented. In Section V, we use temperature-dependent measurements and pulsed I-V measurements to analyze the results from transistors. Finally, we draw some conclusions in Section VI.

II. HETEROSTRUCTURE AND STRAIN ENGINEERING

Most of the work in the field of Sb-channel transistors so far has been on Schottky-gate heterostructure FETs.[7,14] Increasing the transconductance and performance in these transistors requires bringing the gate contact closer to the channel, which causes an exponential increase in current through the Schottky-gate. A MOSFET device with a good gate dielectric that will minimize the leakage current while having a low density of interface states (D_{it}), is direly needed for the antimonides. Also, in these HEMT like devices, the performance is limited by the access resistance arising in part from the large source/drain separation, especially in scaled devices. Although devices with gate lengths down to the nanometer scale have been demonstrated, the source/drain separation has remained comparatively large due to the use of alloyed contacts. Forming the source and drain by ion implantation will help in scaling the pitch of these devices and reducing their access resistance. Such self-aligned designs also make achieving enhancement mode operation much easier.

Thus, in this paper, we report on the fabrication and investigation of MOSFET devices with Al_2O_3 gate dielectric and source and drain formed by ion implantation that are self-aligned with respect to the gate. Figure 1 shows the three different designs of MOSFETs that were fabricated for this work. First, devices on GaSb substrates were studied to optimize the interface with Al_2O_3 and to investigate the diode by analysis of its capacitance-voltage and I-V characteristics.[15] The top surface was terminated with two monolayers of GaSb in all subsequent structures to maintain the high quality interface with Al_2O_3. Second, we explore the use of a thin $In_xGa_{1-x}Sb$ channel on a wide bandgap $Al_{0.80}Ga_{0.20}Sb$ metamorphic buffer grown on GaAs to induce strong confinement that is one contributor to the high mobility. It also serves to reduce I_{OFF} due to the junction leakage from the large source/drain contacts. This is analogous to the use of fully-depleted silicon-on-insulator material for silicon MOSFETs. And third, we study buried channel devices with a thin, wide bandgap $Al_{0.80}In_{0.20}Sb$ cap in order to isolate out the effects of surface roughness and charge in the dielectric on the inversion charge in the $In_xGa_{1-x}Sb$ channel. The wide bandgap $Al_{0.80}In_{0.20}Sb$ layer was kept intentionally thin ($\sim$3–4 nm) so as to avoid any spillover of charge from the channel layer with high mobility into the wide bandgap layer with low mobility.

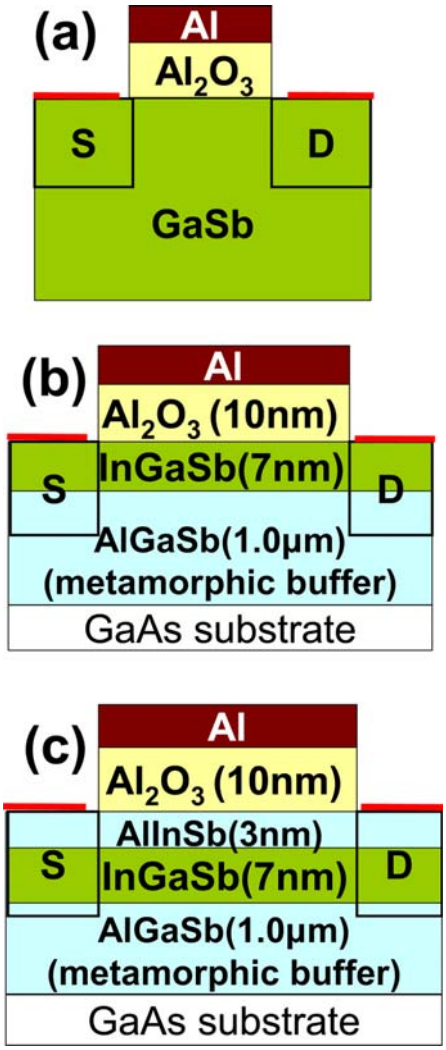

FIG. 1. (Color online) Different transistor designs: (a) A bulk GaSb MOSFET was used to optimize the dielectric interface with GaSb and the diode for source/drain. The top surface was terminated with 2 monolayers of GaSb in all subsequent designs. (b) A heterostructure design with thin InGaSb channel on wide bandgap AlGaSb buffer is used to introduce biaxial strain to improve I_{ON} and cut down drain to body leakage to reduce I_{OFF}. (c) A buried channel design with a thin wide bandgap AlInSb layer between the channel and dielectric is explored to insulate the channel charge from the effect of traps and scattering in the dielectric/III-V interface.

The heterostructures were grown by molecular beam epitaxy (MBE) on a GaAs substrate. The $Al_{0.80}Ga_{0.20}Sb$ buffer is $\sim$1.0 μm thick and accommodates the lattice mismatch of the substrate. Further details on the growth conditions are given in Ref. 5. The thickness of the $In_xGa_{1-x}Sb$ channel was 7.5 nm. $In_xGa_{1-x}Sb$ is known to have residual p-type concentration if undoped;[5] to overcome this residual doping, the $In_xGa_{1-x}Sb$ channel was intentionally doped with Te with a nominal concentration of $1 \times 10^{17}/cm^3$. This resulted in highly resistive p-type samples with sheet resistance $> 80\,000\ \Omega$/square. A biaxial compressive strain of 0.7% or 1.7% was added to the design by increasing the indium fraction in the channel from $In_{0.20}Ga_{0.80}Sb$ to $In_{0.35}Ga_{0.65}Sb$, which increases the lattice constant of the channel with respect to the $Al_{0.80}Ga_{0.20}Sb$

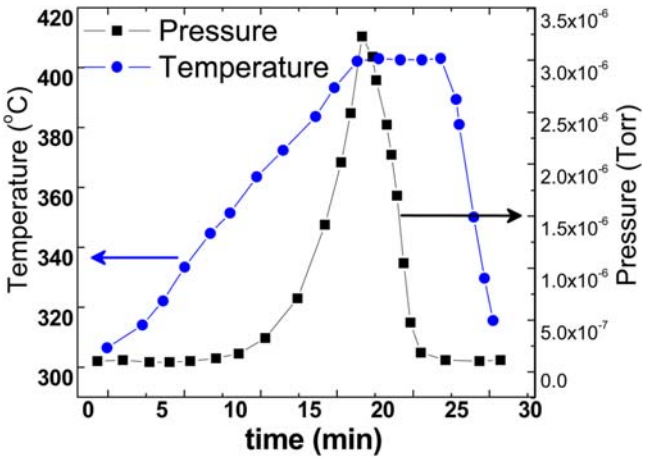

FIG. 2. (Color online) The decapping of the arsenic layer, which is used to prevent the oxidation at the surface, is detected by monitoring the chamber pressure while raising temperature. The chamber temperature is reduced to 300 °C after the arsenic layer is decapped to start the ALD process.

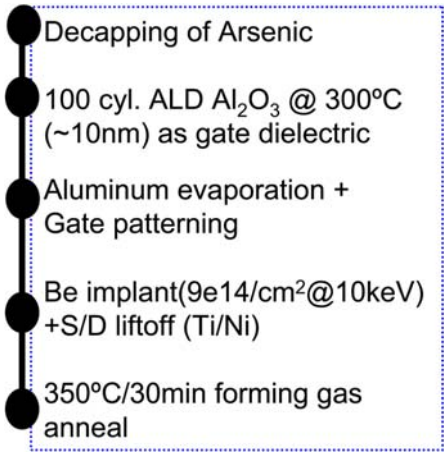

FIG. 3. (Color online) Process flow for fabrication of $In_xGa_{1-x}Sb$ channel pMOSFETs. The maximum temperature during the entire process does not exceed 400 °C.

buffer to further enhance the hole mobility and I_{ON}. The amount of strain present was quantified using high-resolution x-ray diffraction measurements. The buffer was measured to be 97-98% relaxed using reciprocal lattice scans, and the channel was verified to be pseudomorphically strained with respect to the buffer.

III. FABRICATION DETAILS

Following MBE growth, the substrates were capped with ~50 nm of arsenic, a process that has previously been shown effective for preventing the oxidation of the MBE layers due to exposure to the atmosphere.[16] The arsenic capping is then removed under vacuum in the atomic layer deposition (ALD) chamber prior to gate oxide deposition. The decapping of the arsenic can be observed by monitoring the pressure in the ALD chamber versus temperature, as plotted in Fig. 2. As the temperature of the chamber rises to about 400 °C, a spike in the chamber pressure is observed due to decapping of the arsenic that lasts 8-10 mins, after which, the pressure falls back to its original value, indicating the arsenic decapping is complete. The temperature of the chamber is then reduced to 300 °C for the ALD deposition. This arsenic protection step minimizes the exposure of the Sb-surface to air and is critical for obtaining good interface quality.

The MOSFETs were fabricated using a self-aligned gate-first process flow with the different processing steps depicted in Fig. 3. After arsenic decapping, 100 cycles (~10 nm) of ALD Al_2O_3 were deposited at 300 °C for use as the gate dielectric, followed by evaporation and patterning of the aluminum gate material. This was followed by ion implantation of beryllium, which acts as an acceptor in the antimonides. The source and drain contacts were formed by Ti/Ni deposition and lift-off. Fabrication of the transistors was completed with a 350 °C forming gas anneal, which also activates the source/drain implant. The temperature during the entire process never exceeds 400 °C. The low temperature required for source/drain activation allows for a self-aligned gate-first process flow while preserving the high quality at the Al_2O_3/GaSb interface.

Figure 4 shows the cross sectional TEM images for a completed buried channel heterostructure MOSFET. Figure 4(b) shows a high resolution transmission electron micrograph (HR-TEM) near the gate stack; sharp interfaces between the different layers and good crystal quality are maintained after MOSFET processing. An atomically-abrupt interface between the Al_2O_3 and the semiconductor can be observed in the magnified HRTEM image in Fig. 4(c). Also observable in the latter image are the 2 monolayers of GaSb that maintain optimized interface quality while not being so thick as to provide a parallel conduction path.

IV. TRANSISTOR RESULTS

In this section, we discuss the device results obtained on the three types of MOSFETs with emphasis on the effect of the heterostructure design and strain in the channel on the transistor performance. Figure 5 compares the I_D-V_G characteristics of the bulk transistor with the surface channel heterostructure MOSFET. The I_{ON} for the heterostructure design is higher than for the bulk GaSb design because of the use of compressive strain and confinement in the channel. At the same time, we observe an order of magnitude reduction in the I_{OFF} due to much lower body leakage from the large drain contact.

Figure 6 plots the typical output and transfer characteristics for the surface channel heterostructure MOSFET with gate length of 5 μm. The I_{ON}/I_{OFF} is greater than 4 orders of magnitude, and gate current (I_G) and body leakage (I_{SUB}) remain orders of magnitude lower as compared to source/drain current (I_D/I_S) throughout the range of device operation. The subthreshold slope (SS) was measured to be ~120 mV/decade

Figure 7(a) compares the I_D-V_G characteristics of the buried and surface channel devices. A 30% increase in I_{ON} is observed in the buried channel device as compared to the surface channel design. A further 80% increase is obtained with a 1% increase in compressive strain in the channel for

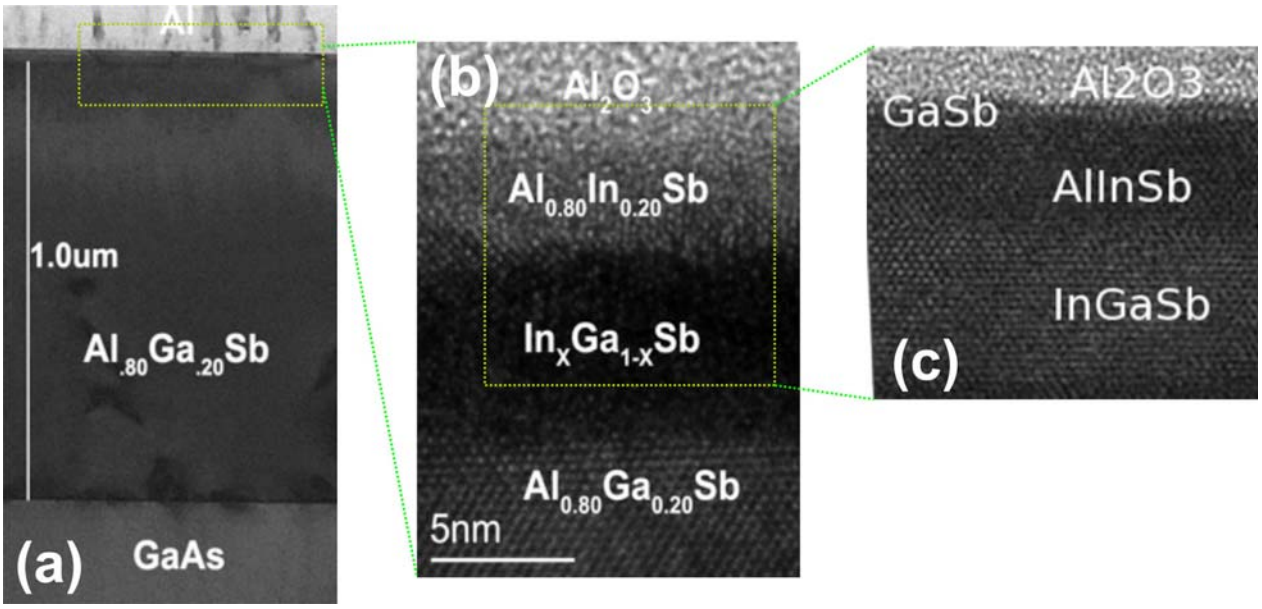

FIG. 4. (Color online) Cross section TEM on the buried $In_xGa_{1-x}Sb$ channel heterostructure MOSFET. (a) 1.0 μm AlGaSb metamorphic buffer absorbs the lattice mismatch with the GaAs substrate. (b) Sharp interfaces between different layers and good crystal quality is maintained after device fabrication. (c) HRTEM shows sharp transition from amorphous oxide to crystalline semiconductor with 2 monolayers of GaSb intact at the semiconductor surface.

both the surface and buried channel designs that is achieved by changing the indium content of the channel from 20% to 35%.

The mobility for these transistors was extracted using a split-CV analysis based on the I_D-V_G characteristics of the transistors (gate length = 25 μm) and the gate-to-channel capacitance (C_{GC}) measured at 100 kHz.[17] Note that no corrections for source/drain resistance or any other corrections were applied while extracting the mobility. Figure 8 plots the extracted mobility and benchmarks it against the known values in unstrained silicon and germanium. We observe that, with 0.7% compressive strain, hole mobility in the surface channel device is higher than silicon over the entire sheet charge range, while for the buried channel device, the mobility remains higher as compared to germanium (Fig. 8(a)). Peak hole mobility in the surface (buried) $In_{0.35}Ga_{0.65}Sb$ channel with 1.7% biaxial compression is more than 300% (400%) higher than for germanium, and the mobility gain is maintained over the entire sheet charge range (Fig. 8(b)). For 1.7% compressive strain, the mobility in the buried (surface) channel device is more than 100% (50%) higher than germanium, even at a sheet charge of $7 \times 10^{12}/cm^2$. The enhancement of hole mobility in the buried channel device over the surface channel configuration is maintained even at high sheet charge thanks to the small thickness and high valence band offset (0.32 eV[11]) of the $Al_{0.80}In_{0.20}Sb$ cap with the channel that prevents the spillover of charge from the high mobility $In_xGa_{1-x}Sb$ channel into the low-mobility capping layer.

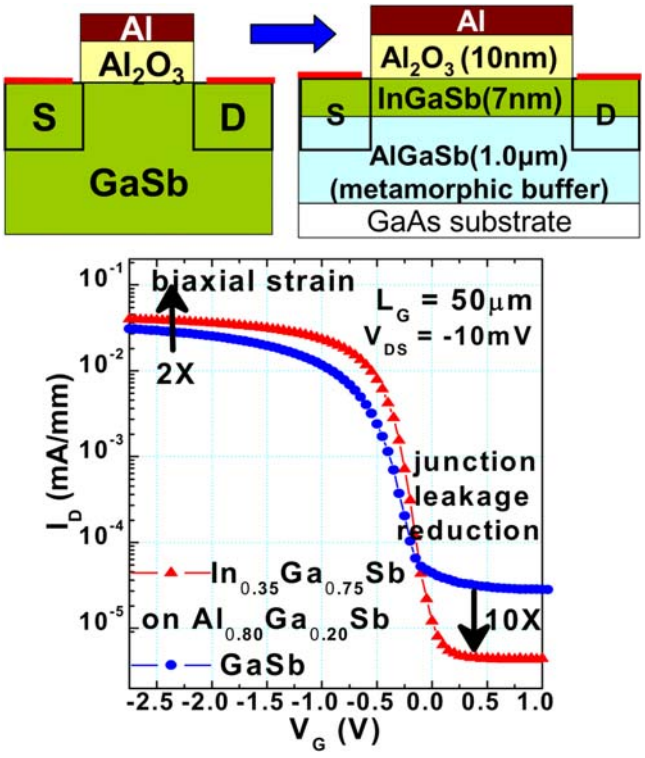

FIG. 5. (Color online) Comparing the I_D-V_G from bulk vs heterostructure design: I_{ON} is increased with the use of strain and confinement, while I_{OFF} is reduced by an order of magnitude due to reduction of body leakage from the drain contact.

The effect of uniaxial strain was studied using wafer-bending experiments.[18,19] The sample was thinned down and bonded to a steel plate as shown in Fig. 9(a). A strain gauge was mounted on top of the sample to measure the strain induced at the top of the III-V surface by the bending. We observed a 4.3% increase in I_D when 50 MPa of uniaxial compression was applied by wafer bending to an $In_{0.35}$ $Ga_{0.65}Sb$ device with the channel oriented along [110] direction (Fig. 9(b)). This gives a piezoresistance coefficient (π_L) of +0.86/GPa, which is higher than the corresponding π_L values of +0.48/0.71/GPa for germanium/silicon pMOSFETs,[20,21]

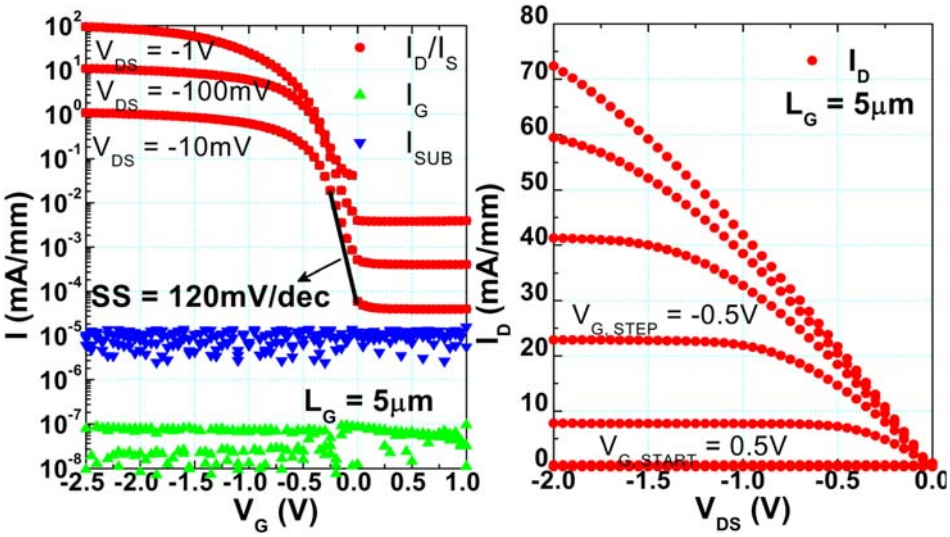

FIG. 6. (Color online) I_D-V_G and I_D-V_D characteristics for surface channel $In_{0.35}Ga_{0.65}Sb$ heterostructure MOSFET. I_{ON}/I_{OFF} is $> 10^4$ and SS is 120 mV/decade.

indicating that an even higher enhancement is possible with further addition of uniaxial strain. Furthermore, the piezoresistance coefficient (π_L) of +0.86/GPa for uniaxial compression is higher than π_L of +0.67/GPa calculated for biaxial compression, indicating that uniaxial strain is more effective in hole mobility enhancement as compared to biaxial strain, a finding that is in line with the theoretical calculations in Ref. 11, as well as with work in silicon/germanium. Regrowth of source/drain can be effectively used to introduce uniaxial strain in short channel III-V MOSFETs[22] similar to uniaxial strain engineering in silicon pMOSFET.[23]

V. ANALYSIS AND DISCUSSION

In this section, we analyze the physics associated with various MOSFET designs. Pulsed IV measurements, in which a voltage pulse is applied on the gate as compared to a DC sweep, were used to estimate the inherent performance of the device (Fig. 10(a)). The rise time, fall time, and width of the pulse were 1 μs, 1 μs, and 20 μs, respectively. Pulsing the gate voltage eliminates the influence of bulk traps and slow interface states on I_{ON} and on mobility.[24] We observe in the Fig. 10(b) that the pulsed IV characteristics show only

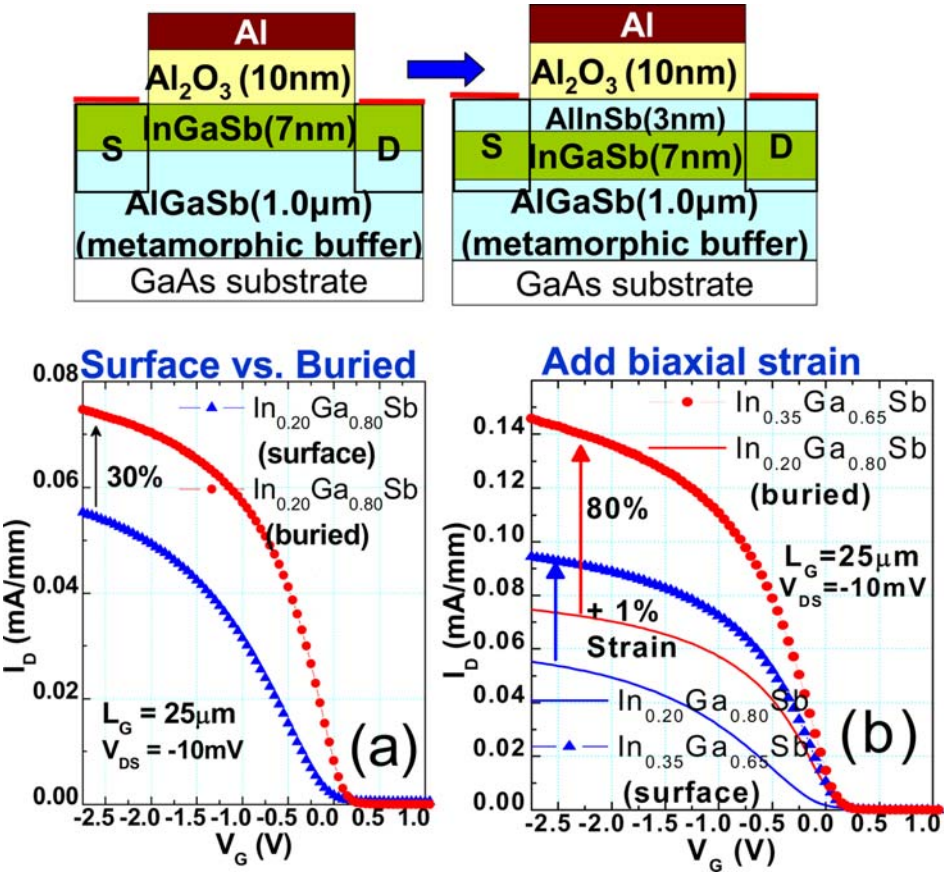

FIG. 7. (Color online) I_D-V_G: (a) comparison between buried and surface channel designs; (b) effect of adding 1% biaxial compression.

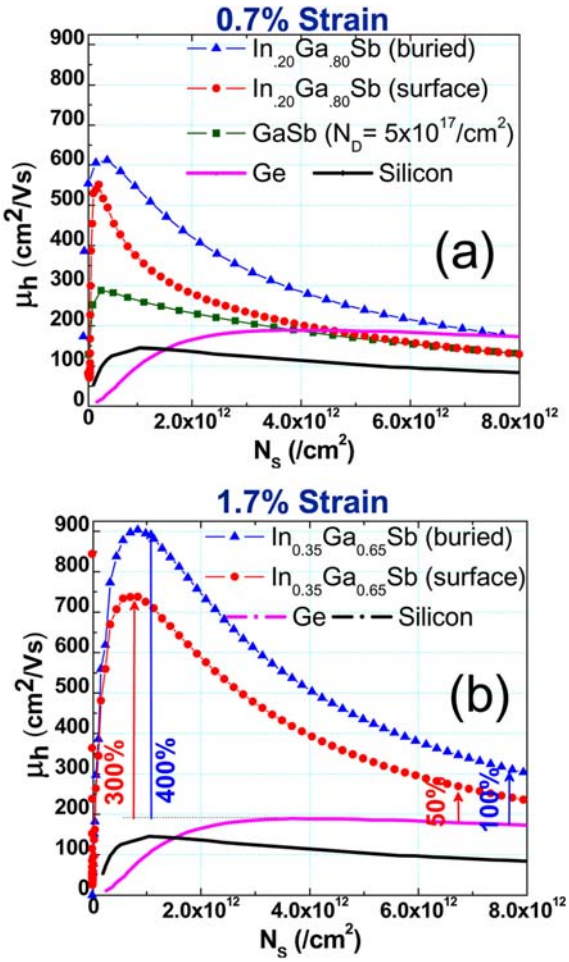

FIG. 8. (Color online) Hole mobility is extracted as a function of sheet charge, using the split-CV technique, and benchmarked against known values in silicon and germanium.

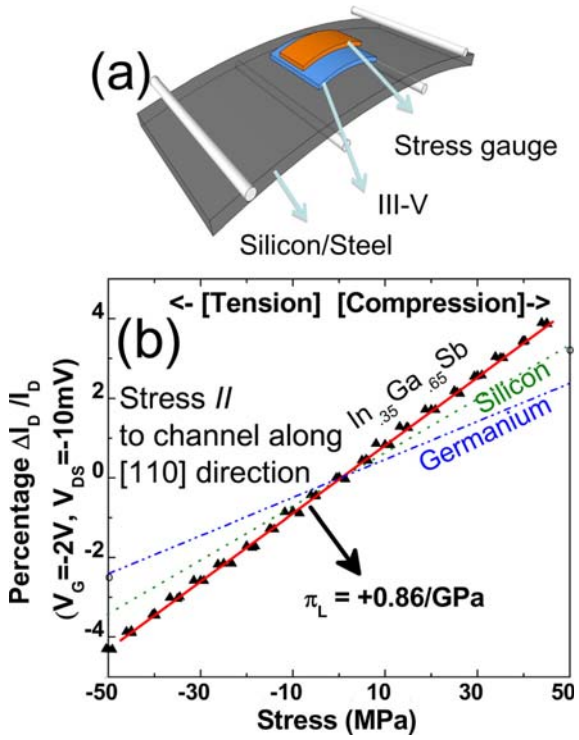

FIG. 9. (Color online) (a) Wafer bending setup used for studying the response of uniaxial strain. (b) 4.3% increase in current is observed with 50 MPa of uniaxial compression, corresponding to a piezoresistive coefficient (π_L) of +0.86/GPa.

a 5% increase over the DC characteristics for the surface channel device, and this reduces to 2% for the buried channel device, suggesting that the influence of traps is minimal in both of our designs.

Figure 11 plots I_D-V_G as a function of temperature. We observe that, as the temperature decreased from 300 K to 80 K, I_{ON} increased up to 4 times due to the increase in the hole mobility, while I_{OFF} decreased by a factor of 10^3, indicating a diode with low defect density. We also monitored the subthreshold swing as a function of temperature in Fig. 11(b) and observed it to scale linearly with temperature from 120 mV/decade at 300 K down to 31 mV/decade at 80 K, providing additional evidence that the effect of traps and interface states is minimal in our devices.

The temperature dependence of hole mobility was studied for both the surface and buried channel devices, as plotted in Fig. 12. We observe a higher increase in mobility with the lowering of temperature in the buried channel device as

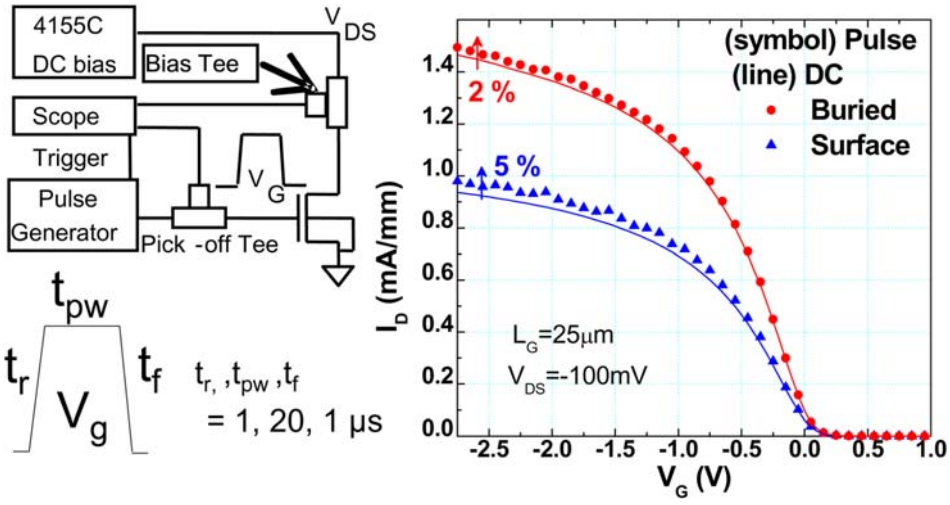

FIG. 10. (Color online) Pulse IV measurements were carried out on both buried and surface channel MOSFETs. 5%/2% improvements over the DC characteristics were observed with pulse IV for the surface/buried design.

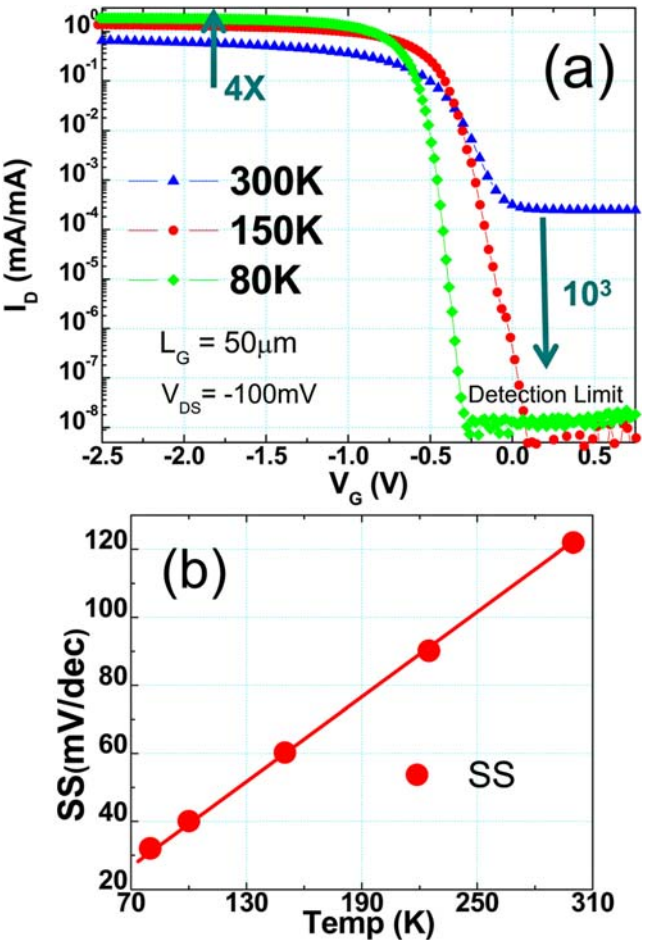

FIG. 11. (Color online) As the temperature is reduced from 300 K to 80 K: (a) I_{ON} increases by 4 times, while I_{OFF} decreases by 3 orders in magnitude; (b) the subthreshold swing (SS) decreases linearly as a function of temperature.

compared to the surface channel device. The temperature dependence at a fixed sheet charge density of $5 \times 10^{12}/cm^2$ is compared in Fig. 13. Temperature dependence of T^{-1} characteristic of mobility limited by interface roughness scattering[25] is observed for the surface channel device. For the buried channel device, a temperature dependence of $T^{-1.32}$ is observed, which is closer to the $T^{-1.5}$ dependence associated with mobility limited by phonon scattering.[25] This suggests that the mobility gain in the buried channel device is primarily due to suppression of scattering from the interface roughness at the oxide/semiconductor interface. The root mean square roughness values achieved on the GaSb surface and the known values in silicon/germanium are summarized in Table I. We do observe higher roughness in our devices as compared to silicon/germanium.

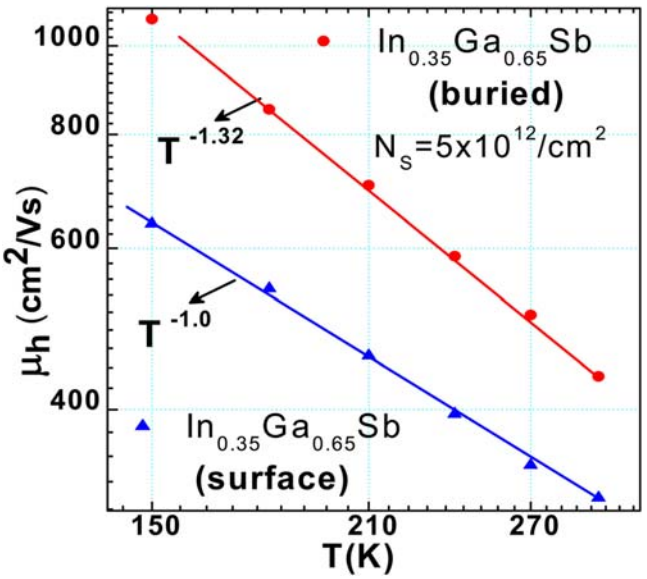

FIG. 13. (Color online) Hole mobility is plotted as a function of temperature at fixed sheet charge density of $5 \times 10^{12}/cm^2$. Temperature dependence of T^{-1} characteristic of mobility limited by interface scattering is observed for the surface channel design. The temperature dependence is $T^{-1.32}$ for the buried channel design.

A potential concern for transistors made with III-V materials is the high band-to-band tunneling (BTBT) leakage current due to the direct bandgap and smaller bandgap in III-V's as compared to silicon. Krishnamohan *et al.*[26] predicted through simulations that this BTBT can limit the minimum achievable I_{OFF} in these transistors, especially at scaled gate lengths. At low temperature, when I_{ON}/I_{OFF} becomes $> 10^8$, gate induced drain leakage (GIDL) due to BTBT was observed in the surface channel device, as plotted in Fig. 14. No similar signature of GIDL due to BTBT was observed in the buried channel device. The reason for this is clear from a plot of the electric field profile at high drain-to-gate bias (V_{DG}) obtained using 2D technology computer-aided design (TCAD) simulation in Fig. 14(b). In particular, the maximum

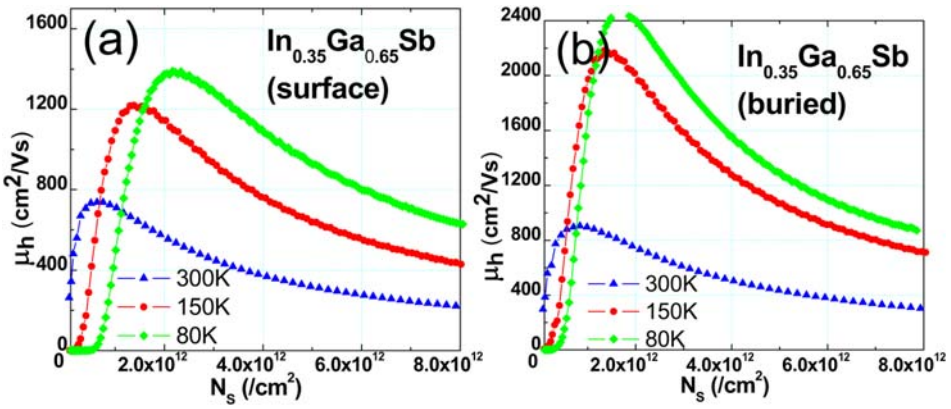

FIG. 12. (Color online) Hole mobility with varying temperature for (a) surface (b) buried channel MOSFET. Buried channel device exhibits higher increase in mobility with lowering in temperature as compared to the surface channel design.

TABLE I. Surface roughness comparison with known values in silicon and germanium MOSFETs.

(100) Surface	Sb's	Si	Ge
Pre-clean	0.36 nm	0.28 nm	0.15 nm
After oxide clean/10 cycles ALD	0.73 nm	0.41 nm (Ref. 27)	0.11 nm (Ref. 27)

electric field in the buried channel device moves as a result of V_{GD} into the wide bandgap $Al_{0.80}In_{0.20}Sb$ cap, thereby suppressing the BTBT. Thus, the buried channel device is effective in suppressing BTBT, which might be the dominant component of I_{OFF} in scaled devices.[26]

VI. CONCLUSION

The use of an arsenic cap that is removed in vacuum prior to ALD dielectric deposition is found to prevent oxidation of the Sb-surface and give an atomically abrupt interface with the gate oxide that is key for obtaining good interface quality. A self-aligned process flow was designed for MOSFET fabrication, where the maximum temperature during the entire process flow does not exceed 400 °C. Table II summarizes the key transistor results. We demonstrated $In_xGa_{1-x}Sb$ pMOSFETs with subthreshold slope of 120 mV/decade, $I_{ON}/I_{OFF} > 10^4$ and $G_{m,max}$ of 140/90 mS/mm for a gate length of

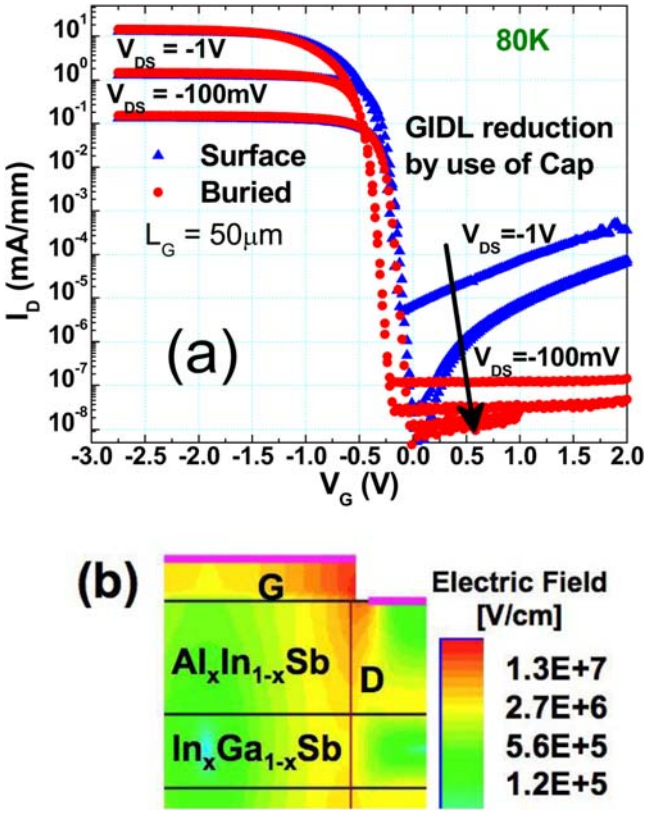

FIG. 14. (Color online) (a) GIDL due to BTBT is observed in the surface channel device at 80 K, while the buried channel design shows no such signature. (b) The maximum electric field between the gate and drain in the buried channel device occurs in the wide bandgap $Al_xIn_{1-x}Sb$ layer, suppressing BTBT.

TABLE II. Summary of results.

Sample	SS (mV/dec)	$\mu_{h,peak}$ (cm^2/Vs)	$\mu_h N_S = 5 \times 10^{12}$	$G_{m,max}$ $L_G = 5$ μm	I_{ON}/I_{OFF}	Biaxial strain
Surface ($In_{0.35}Ga_{0.65}Sb$)	120	620	320	94 mS/mm	$> 10^4$	1.7%
Buried ($In_{0.35}Ga_{0.65}Sb$)	125	910	435	140 mS/mm	$> 10^4$	1.7%

5 μm. Excellent subthreshold slope and marginal difference between the pulse IV and DC IV measurements revealed excellent interface quality.

The use of biaxial strain was successful in improving transistor performance, where an 80% improvement in I_{ON} was observed with the addition of 1% biaxial compression. The effect of uniaxial strain was studied using wafer-bending experiments. A 4.3% increase in I_{ON} was observed with the addition of just 50 MPa of uniaxial compression, suggesting further enhancement in transistor performance should be possible with uniaxial strain engineering.

Both surface channel devices and buried channel device with a thin wide bandgap layer between the channel and oxide were studied. The buried channel device exhibited a 30% improvement in I_{ON} over the surface channel device. Temperature dependence study of IV characteristics and hole mobility revealed that this improvement was mainly due to reduction of carrier scattering at the oxide interface. The buried channel design is also effective in reducing the BTBT leakage. In conclusion, we have demonstrated buried (surface) InGaSb pMOSFETs with peak hole mobility of 910 (620) cm^2/Vs and having more than 100 (50)% mobility gain on germanium over the entire sheet charge range.

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