Abstract—While there have been many demonstrations on n-channel metal–oxide–semiconductor field-effect transistors (MOSFETs) in III–V semiconductors showing excellent electron mobility and high drive currents, hole mobility in III–V p-channel MOSFETs (pMOSFETs) has traditionally lagged in comparison to silicon. GaSb is an attractive candidate for high-performance III–V pMOSFETs due to its high bulk hole mobility. We fabricate and study GaSb pMOSFETs with an atomic layer deposition Al₂O₃ gate dielectric and a self-aligned source/drain formed by ion implantation. The band offsets of Al₂O₃ on GaSb were measured using synchrotron radiation photoemission spectroscopy. The use of a forming gas anneal to passivate the dangling bonds in the bulk of the dielectric was demonstrated. The density of interface states \( D_{\text{it}} \) was measured across the GaSb band gap using conductance measurements, and a midband-gap \( D_{\text{it}} \) of \( 3 \times 10^{12} \) \( \text{cm}^{-2}\text{eV}^{-1} \) was achieved. This enabled pMOSFETs with a peak hole mobility value of 290 \( \text{cm}^2/\text{Vs} \).

Index Terms—Atomic layer deposition (ALD), gallium antimonide, hole mobility, III–V p-channel metal–oxide–semiconductor field-effect transistors (pMOSFETs).

I. INTRODUCTION

GaSb is an exciting III–V material, which may enable a high-performance/low-power complementary metal–oxide–semiconductor (CMOS) technology, which can outperform silicon. While there have been many demonstrations on n-channel metal–oxide–semiconductor field-effect transistors (nMOSFETs) in III–V showing excellent electron mobility and high drive currents, hole mobility in III–V p-channel MOSFETs (pMOSFETs) has traditionally lagged in comparison to silicon. GaSb is an attractive material for pMOSFET due to its high bulk hole mobility. We fabricate and study GaSb pMOSFETs with an atomic layer deposition Al₂O₃ gate dielectric and a self-aligned source/drain formed by ion implantation. The band offsets of Al₂O₃ on GaSb were measured using synchrotron radiation photoemission spectroscopy. The use of a forming gas anneal to passivate the dangling bonds in the bulk of the dielectric was demonstrated. The density of interface states \( D_{\text{it}} \) was measured across the GaSb band gap using conductance measurements, and a midband-gap \( D_{\text{it}} \) of \( 3 \times 10^{12} \) \( \text{cm}^{-2}\text{eV}^{-1} \) was achieved. This enabled pMOSFETs with a peak hole mobility value of 290 \( \text{cm}^2/\text{Vs} \).

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explored the use of in situ deposition of Al$_2$O$_3$ on GaSb grown on InP using molecular beam epitaxy and reported $D_{it}$ values in the low $10^{13}$/cm$^2$eV range near the valence band [8]. While these are exciting results, the development of high-quality ALD dielectric on the GaSb surface still remains a nascent field, and MOSFETs on GaSb utilizing the ALD dielectric and their mobility have not been reported yet. In this paper, we explore the use of thermal ALD Al$_2$O$_3$ to achieve quality MOSFETs with a GaSb channel.

Another challenge in achieving high-performance MOSFETs on GaSb is the development of source/drain technology with high density of activated carriers, low defects, and low contact resistance. Ion implantation in antimonides has traditionally been a challenge; the formation of hillocks and voids has been well known with high-dose of ion implantation in GaSb [9], [10]. In this paper, we attempt to overcome these challenges and demonstrate a pMOSFET in GaSb substrate using ALD Al$_2$O$_3$ as the dielectric and source/drain formed by ion implantation in a self-aligned process flow.

The rest of this paper is organized as follows: In Section II, we report on the development of an Al$_2$O$_3$ gate dielectric on GaSb. Capacitance/conductance measurements and radiation from synchrotron are used to study the dielectric properties. The use of a forming gas anneal (FGA) to improve the dielectric properties is also discussed. Section III details the ion implantation process for forming source/drain and $p^+/n$ diode characteristics for the pMOSFET. Section IV describes the fabrication flow and results obtained on the fabricated GaSb pMOSFET devices. Finally, we draw some conclusions in Section V.

II. DIELECTRIC DEVELOPMENT

A high-quality dielectric on the GaSb surface is the key for achieving good MOSFET characteristics. Here, we report on the optimization of ALD Al$_2$O$_3$ for the GaSb surface. We choose Al$_2$O$_3$ as it has the advantages of a large band gap, high dielectric constant, high breakdown field ($> 10^7$ V/cm), and thermal stability (amorphous for temperatures up to 1000 °C). The amorphous Al$_2$O$_3$ film also acts as a better barrier for alkali ions, has fewer impurities, and has higher radiation resistance. Any high-$k$ oxide for a III–V MOSFET must satisfy two basic criteria, i.e., 1) a clean and native-oxide-free interface with the semiconductor and 2) sufficient band offset of over 1 eV to act as a barrier for both electrons and holes [1]. The GaSb surface has been known to be highly reactive to atmospheric oxygen, and a thick native oxide quickly forms on the surface [11]. The removal of this oxide to produce a clean and thermally stable surface is essential in achieving good interface quality and low density of interface states $D_{it}$. We use a chemical clean in 1:1 HCl for surface preparation before ALD. A HCl acid-based clean is effective to remove both the GaO$_x$ and SbO$_y$ on the GaSb surface. The comparison of various chemical cleans in producing a device-quality Sb surface was extensively studied using low-energy synchrotron radiation and photoluminescence measurements and has been reported elsewhere [12]. After the chemical clean, Al$_2$O$_3$ was deposited at 300 °C by ALD using trimethyl aluminum (TMA) and water as the precursors with TMA being the starting pulse for the ALD. The root-mean-square (RMS) roughness values of the surface just after HCl clean and after 10 cycles of ALD deposition were measured to be 0.66 and 0.73 nm, respectively, as shown in Fig. 1.

Synchrotron radiation photoemission spectroscopy (SRPES) was used to estimate the conduction band offset (CBO) and the valence band offset (VBO) for Al$_2$O$_3$ on GaSb. The Al$_2$O$_3$ band gap was measured to be 6.3 eV from the Al 2p loss spectrum [see Fig. 2(a)], which agrees well with values reported for ALD Al$_2$O$_3$ deposited under similar conditions [13]. The VBO was measured by taking the difference between the valence band spectrum from the surface after the clean and after thin Al$_2$O$_3$ deposition, as shown in Fig. 2(b) [14], using the Sb 4d peak from the GaSb substrate for alignment [see Fig. 2(c)]. The VBO was measured to be 3.1 eV by SRPES, which has a high-energy resolution near the valence band spectrum maximum. Using the known value of the GaSb band gap (0.72 eV) at room temperature, the CBO can be estimated by taking the difference of the Al$_2$O$_3$ band gap with the VBO and the GaSb band gap, as shown in Fig. 3. The measured CBO/VBO of 2.48 eV/3.1 eV for Al$_2$O$_3$ on GaSb are sufficient to minimize gate leakage by thermionic and tunneling processes, and the insulator is therefore well suited for a MOSFET design.

Al$_2$O$_3$ films with thicknesses of 5–15 nm were deposited on GaSb using ALD. Film thickness was measured using ellipsometry, which was also verified with cross-sectional transmission electron microscopy. Capacitors were made on these films using platinum (Pt) electrode deposited in an e-beam evaporator through a shadow mask. Fig. 4(a) plots the capacitance–voltage (CV) characteristics as a function of oxide thickness for the as-deposited dielectric. We use a chemical clean in 1:1 HCl for surface preparation before ALD. A HCl acid-based clean is effective to remove both the GaO$_x$ and SbO$_y$ on the GaSb surface. The comparison of various chemical cleans in producing a device-quality Sb surface was extensively studied using low-energy synchrotron radiation and photoluminescence measurements and has been reported elsewhere [12]. After the chemical clean, Al$_2$O$_3$ was deposited at 300 °C by ALD using trimethyl aluminum (TMA) and water as the precursors with TMA being the starting pulse for the ALD. The root-mean-square (RMS) roughness values of the surface just after HCl clean and after 10 cycles of ALD deposition were measured to be 0.66 and 0.73 nm, respectively, as shown in Fig. 1.

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Fig. 2. (a) Band gap $E_g$ of Al$_2$O$_3$ is measured using the Al 2p loss spectrum. (b) VBO is measured by taking the difference between the valence spectrum before and after depositing a thin layer of Al$_2$O$_3$. (c) While using the Sb 4d peak from the substrate for alignment.

$V_{FB}$ was extracted using the method of Hillard et al. [16]. The observed thickness dependence of $V_{FB}$ can be explained if we assume that there is negative fixed charge near the Al$_2$O$_3$ interface with GaSb and positive charge in the bulk of the oxide film. A negative linear shift in $V_{FB}$ as a function of dielectric thickness occurs due to negative charge at the semiconductor/oxide interface, as shown in Fig. 5, whereas a positive parabolic shift is expected when there is positive bulk charge present in the dielectric [17]. The functional dependence of the measured data can be fitted very well with the combination of negative linear and positive parabolic dependence (see Fig. 5), confirming the presence of positive bulk charge in the oxide and negative charge at the oxide/GaSb interface for the as-deposited Al$_2$O$_3$. A similar charge distribution has been also observed for Al$_2$O$_3$ on InGaAs deposited under similar conditions by Shin et al. [18]. The authors attributed this charge distribution to the presence of an O-rich region near the interface and an Al-rich region away from the interface. It is known from first-principle calculations in amorphous Al$_2$O$_3$ that the Al deficiency manifests itself in the form of oxygen dangling bonds,
which have charge-transition levels at $-0.83$ and $0.61$ eV above the valence band, as shown in Fig. 3, whereas the aluminum dangling bonds due to O deficiency are located at $5.12$ and $5.35$ eV above the valence band (see Fig. 3) [18].

Looking at the position of these dangling bonds in Fig. 3, we can predict that the O dangling bonds will be below the Fermi level and thus will be negatively charged, whereas the Al dangling bonds will be positively charged. This agrees well with the experimental result that the O-rich region near the interface has fixed negative charge, whereas the Al-rich region in the bulk has positive charge.

As the presence of fixed charge in the oxide or at the oxide/semiconductor is detrimental for MOSFET performance, the use of FGA was explored to reduce the fixed charge and improve the Al$_2$O$_3$/GaSb interface properties. Recently, the use of FGA has been shown to be very effective at improving the interface properties of the oxide/In$_x$Ga$_{1-x}$As interface and passivating the bulk traps in Al$_2$O$_3$ deposited by ALD under similar conditions [18], [19]. A theoretical analysis has predicted binding energy values of $1.3$ eV for O–H and $1.4$ eV for Al–H indicative of stable passivation. Hydrogen passivation can hence neutralize the effect of dangling bonds and improve the interface properties. Motivated by this, we tried an FGA anneal with forming gas ($5/95\% : \text{H}_2/\text{N}_2$) flowing at the rate of $\sim4$ L/min at varying temperatures. A $30\text{ min/350 }^\circ\text{C}$ anneal was found to be optimum to improve the dielectric properties. Fig. 4(b) plots the CV characteristics following the FGA anneal, where the normalized CVs for different dielectric thicknesses overlap each other, indicating the removal of fixed charge. The hysteresis reduces from $\sim120$ mV for the as-deposited condition to $\sim20$ mV after the FGA anneal, indicating passivation of bulk traps (see Fig. 4). A reduction in stretch-out indicating reduction of $D_{it}$ was also observed. The temperatures above and below $350$ $^\circ\text{C}$ were found to be less effective in improving the dielectric properties with FGA. A similar behavior with temperature has been observed with the effect of FGA on the dielectric/Ge interface [20] and has been attributed to insufficient diffusion of hydrogen radicals at low temperatures ($<350$ $^\circ\text{C}$) and deterioration of interface properties due to intermixing at the semiconductor/dielectric interface and desorption of hydrogen at higher temperatures ($>350$ $^\circ\text{C}$).

Fig. 6 plots the CV characteristics obtained after the FGA anneal on p- and n-type GaSb substrates for the frequency range of 1–100 kHz. An inversion response at room temperature was observed on both n- and p-type GaSb substrates. Frequency dispersion in accumulation, which is one indicator of $D_{it}$, was less than $1/2.1$/dec for the p- and n-type substrates. The $D_{it}$ distribution across the band gap was determined using the conductance method in the depletion region [21], [22] on n- and p-type substrates. The temperature was varied from $300$ K–$80$ K, and measurements were made on both n- and p-type substrates to probe the $D_{it}$ distribution across the entire band gap. Fig. 7 shows a typical $G_{p}/\omega$ versus frequency curve for the p-type substrate at $77$ K. Fig. 8 plots the derived $D_{it}$ distribution. A midband-gap $D_{it}$ value of $3 \times 10^{11}$/cm$^2$eV was achieved. The $D_{it}$ distribution is asymmetric with low $D_{it}$ near the valence band edge and an order of magnitude higher $D_{it}$ toward the conduction band. The low $D_{it}$ values near the valence band is encouraging for obtaining a good pMOSFET, whereas the high $D_{it}$ values near the conduction band can be detrimental to the nMOSFET performance. It must be noted that the minimum of the $D_{it}$ distribution occurs near the charge neutrality level of GaSb, which is located at $\sim0.1$ eV from the valence band [1]. We also note that the $D_{it}$ distribution obtained is qualitatively similar to what is experimentally observed in germanium, which has a similar band gap as GaSb, and its charge neutrality center is located near the valence band as well [23].

III. DIODE DEVELOPMENT FOR SOURCE/DRAIN

For the development of GaSb pMOSFET source/drain technology with a high density of activated carriers, low defects and low contact resistance are essential. Ion implantation in the antimonides has traditionally been a challenge, as the formation of hillocks and voids with a high dose of implantation in GaSb has been well known [9], [10]. In addition, it has been reported that this damage does not go away with furnace or rapid thermal anneal (RTA) even at high temperature. Furthermore, it has been noted that the threshold dose/energy of hillock formation decreases with increasing ion mass [9], [10]. Table I lists the dopant species for GaSb, i.e., Be, Si, and Zn act as acceptors in GaSb, and S, Se, and Te are the common donors. Thus, for the p$^+/n$ diode, the implantation dose at which hillock formation occurs is on the order of Zn $<$ Si $<$ Be. Similarly, for the n$^+/p$ diode, it is on the order of S $<$ Se $<$ Te. The problem is worse for donors as the lightest atom for donors is S compared to Be for acceptors. It should be also noted that most of the previous work on implantation in GaSb was done without any dielectric layer on the top to absorb the energy of species being implanted.

We experimented with ion implantation of several species in GaSb using thin ($\sim10$ nm) Al$_2$O$_3$ as the capping layer. The selection of implant energy and dose was guided by simulations performed with SRIM software [24] to produce a peak of the dopant species at the surface. Fig. 9(a)–(c) shows the atomic force microscopy (AFM) map of the surface after implantation
IV. TRANSISTOR FABRICATION AND CHARACTERISTICS

GaSb pMOSFETs were fabricated using a self-aligned gate-first process flow on an n-type GaSb substrate grown by the Czochralski process with Te as the n-type dopant. A carrier concentration of \( \sim 3-4 \times 10^{17} / \text{cm}^3 \), which was the lowest available commercially, was chosen to reduce the effect of Coulomb scattering on transistor mobility. One hundred cycles (\( \sim 10 \) nm) of ALD \( \text{Al}_2\text{O}_3 \) were deposited at 300 °C for use as the gate dielectric, followed by evaporation and patterning of the aluminum gate material. This was followed by ion implantation of beryllium. The source and drain contacts were formed by Ti/Ni implantation.

TABLE I

<table>
<thead>
<tr>
<th>Name</th>
<th>Nature</th>
<th>Atomic Mass</th>
</tr>
</thead>
<tbody>
<tr>
<td>Be</td>
<td>Acceptor</td>
<td>9</td>
</tr>
<tr>
<td>Si</td>
<td>Acceptor</td>
<td>28</td>
</tr>
<tr>
<td>Zn</td>
<td>Acceptor</td>
<td>65.4</td>
</tr>
<tr>
<td>S</td>
<td>Donor</td>
<td>32</td>
</tr>
<tr>
<td>Se</td>
<td>Donor</td>
<td>78.9</td>
</tr>
<tr>
<td>Te</td>
<td>Donor</td>
<td>127.6</td>
</tr>
</tbody>
</table>

characteristics are plotted in Fig. 10(a). Good diode characteristics with \( I_{\text{ON}}/I_{\text{OFF}} \) of \( > 5 \times 10^4 \) and an ideality factor of 1.4 could be obtained with annealing at 350 °C, as shown in Fig. 10(b).

Fig. 11 plots the temperature dependence of the reverse leakage current for the p\( ^+ \)/n diode. Reduction in reverse current was observed when the temperature was decreased from 300 K to 80 K. Activation energy \( E_a \) was calculated to be \( \sim 0.33 \) eV from the slope of the observed characteristics in Fig. 11. This value is close to half of the band gap of GaSb (\( E_g \sim 0.72 \) eV), suggesting that the intrinsic generation–recombination is dominant in the reverse leakage current [17], [25], [26].

with Be, S, and Zn, respectively. A significant increase in surface roughness due to implant damage was observed for heavier species such as S and Zn. Furthermore, we observed that the surface still remains rough after RTA [see Fig. 9(d)]. The only good result was on Be, which has the lowest atomic mass and for which the surface roughness was less than 1 nm for an implant dose of \( 9 \times 10^{14} / \text{cm}^2 \). Various implant and anneal conditions were attempted for Be to optimize the p\( ^+ \)/n diode characteristics for the pMOSFET. The obtained diode IV
Fig. 9. AFM scan of the surface after: (a) Be implant with dose $= 9 \times 10^{14} \, \text{cm}^{-2}$ and energy $= 10 \, \text{keV}$; (b) S implant with dose $= 7 \times 10^{14} \, \text{cm}^{-2}$ and energy $= 40 \, \text{keV}$; (c) Zn implant with dose $= 7 \times 10^{14} \, \text{cm}^{-2}$ and energy $= 30 \, \text{keV}$; and (d) RTA anneal of the Zn implanted sample at 600 $^\circ\text{C}$ for 5 min.

Fig. 10. (a) Various implant and anneal conditions were attempted to optimize the diode characteristics. (b) Diode with $I_{ON}/I_{OFF}$ of $5 \times 10^4$, and ideality factor of 1.4 was achieved with annealing at 350 $^\circ\text{C}$.

Fig. 11. Reverse current $J_R$ at applied voltage of $-0.5 \, \text{V}$ is measured as a function of temperature. The activation energy $E_a$ of 0.33 eV is extracted from the slope.

deposition and liftoff. Fabrication of the transistors was completed with a 350 $^\circ\text{C}$ forming gas anneal, which also activates the source/drain implant. The temperature during the entire process never exceeds 400 $^\circ\text{C}$. The low temperature required for source/drain activation allows for a self-aligned gate-first process flow without causing intermixing at the Al$_2$O$_3$/GaSb interface. The sheet resistance in the source/drain regions was measured to be $300 \, \Omega$/$\text{square}$ using the transfer length method. Specific contact resistance of the Ti/Ni source/drain contact was measured to be $\sim 2 \times 10^{-5} \, \Omega\cdot\text{cm}^2$.

Fig. 12 plots the $I_D-V_G$ characteristics for the MOSFET device. The source current ON/OFF ratio is $> 10^4$, whereas the off current for the drain is limited by the reverse leakage through the large drain/body contact at large drain voltages (see
Fig. 12. Output characteristics of the GaSb pMOSFET.

The mobility for these transistors was extracted using the split CV analysis based on the $I_D-V_G$ characteristics of the transistors (gate length = 25 µm) and the gate-to-channel capacitance $C_{GC}$ measured at 100 kHz [17]. Note that no corrections for source/drain resistance or any other corrections were applied while extracting the mobility. Fig. 13 plots the extracted mobility as a function of sheet charge in the channel; a peak field-effect hole mobility of 290 cm$^2$/Vs was obtained. Universal hole mobility in silicon is also plotted for comparison (see Fig. 13); the peak mobility in GaSb MOSFET is approximately twice higher in comparison to silicon, and the mobility gain over silicon is maintained even at high sheet charge. An increase in the ON current and correspondingly the mobility was observed when the temperature was decreased from 300 K to 80 K. The temperature dependence of mobility at a fixed sheet charge density of $5 \times 10^{12}$/cm$^2$ is plotted in Fig. 14. The temperature dependence of $T^{-0.85}$ is observed, which is closer to the $T^{-1.0}$ dependence associated with mobility limited by interface roughness scattering. We did observe higher roughness in our devices, as compared to silicon/germanium from the AFM study in Fig. 1. The surface roughness on the GaSb surface clean was 0.66 nm, which is roughly twice higher in comparison to state-of-art silicon [27]. We believe that further optimization of the transistor output characteristics is possible with further improvement of the diode characteristics using a higher implant dose and an RTA.

V. C ONCLUSION

In conclusion, we have reported on the development of a high-quality ALD Al$_2$O$_3$ gate dielectric on GaSb. The band offsets of Al$_2$O$_3$ on GaSb were measured using SRPES and determined to be suitable for MOSFET development. FGA was effectively used to passivate the dangling bonds in the bulk of the dielectric and also to improve the interface properties [18]–[20]. Excellent CV characteristics were demonstrated on both p- and n-type substrates with frequency dispersion of less than 1/2.1%/dec. The $D_{it}$ distribution was measured across the GaSb band gap using conductance measurements; midband-gap $D_{it}$ of $3 \times 10^{11}$/cm$^2$eV was achieved. A $p^+/n$ diode with an ON/OFF ratio of $5 \times 10^4$ and an ideality factor of 1.4 was demonstrated using ion implantation of Be.

A self-aligned process flow was used for fabricating pMOSFETs with the source/drain formed by ion implantation of Be. The maximum temperature during the process flow does not exceed 400 °C. Good transistor characteristics with $I_{ON}/I_{OFF} > 10^3$ and peak hole mobility of 290 cm$^2$/Vs were obtained. Temperature-dependent measurements revealed a mobility value limited by interface scattering and a defect-free diode. This development paves the way for the demonstration of a complementary technology in III–V materials outperforming silicon.

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Yoshio Nishi (SM’82–F’88) received the B.S. degree in materials science and engineering from Waseda University, Tokyo, Japan, and the Ph.D. degree (thesis doctor) in electronics engineering from the University of Tokyo, Tokyo.

He joined Toshiba Corporation, working in the area of semiconductor materials and processes during which he discovered the ESRR PB Center at the Si–SiO2 interface, which is now accepted as the origin of the fast interface states. He is one of the pioneers in MNOS nonvolatile memory resulting in 256- and 1024-bit MNOS RAM devices productized in early 1970s. He led the group of silicon-on-sapphire (SOS)-based device research in the Research and Development (R&D) Center and developed technology for a 16-bit SOS microprocessor of medical computer for high-speed image data processing. Later, he managed the group of memory technology R&D in the Semiconductor Device Engineering Laboratory, which developed the world’s first 1-Mb CMOS DRAM and 256-Kb SRAM and EPROM. In 1986, he joined Hewlett-Packard (HP) as the Director of the Silicon Process Laboratory, and then, he became the Director for the Integrated Circuit Business Division R&D Center running HP’s high-performance CMOS technology R&D for PA RISC chips. He established the ULSI Research Laboratory as the advanced IC technology research for HP. In 1996, he joined Texas Instruments (TI), Dallas, as a Senior Vice President and the Director of R&D, in which he established a new R&D model and the Kilby Center for TI’s IC technology R&D. In 2002, he joined Stanford University, Stanford, CA, as a Professor of electrical engineering. He served as the Director of Stanford Nanofabrication Facility, and he is currently the Research Director of the Center for Integrated Systems. His research interest at Stanford University includes resistive-change nonvolatile memory devices, new channel materials, including inorganic and organic semiconductors, metal-gate work-function engineering, graphene band engineering, and group IV semiconductor light emissions. He has published more than 250 papers/conference talks, coauthored/edited 12 books, and held more than 50 patents in USA and Japan. Dr. Nishi is the recipient of the IEEE Jack Morton Award (1995), the IEEE Robert Noyce Medal (2002), the PICMET Leadership in Technology Management Award (2007), and the SEMI Lifetime Achievement Award (2008).

Krishna C. Saraswat (M’70–S’71–SM’85–F’89) received the B.E. degree in electronics from Birla Institute of Technology and Science, Pilani, India, in 1968 and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1969 and 1974, respectively.

After finishing his Ph.D., he stayed at Stanford University as a Researcher and was appointed as a Professor of electrical engineering in 1983. He is currently a Rickey/Nielsen Professor, and by courtesy, a Professor of materials science and engineering with the School of Engineering, Stanford University. During 1969–1970, he was with Texas Instruments, Dallas, where he worked on microwave transistors. He serves in the Leadership Council of the MARCO/DARPA-funded Focus Center for Materials, Structures, and Nano-Devices. He also has an honorary appointment of being an Adjunct Professor with Birla Institute of Technology and Science since January 2004 and a Visiting Professor during the summer of 2007 with the Indian Institute of Technology Bombay, Mumbai, India. During 2000–2007, he was an Associate Director of the NSF/SRC Center for Environmentally Benign Semiconductor Manufacturing. He has been a technical advisor, board member, and consultant to several industrial organizations in USA, Asia, and Europe. He has also advised several academic and government organizations worldwide. He was able to make more than 70 doctoral students graduate. He is the author or coauthor of more than 650 technical papers and the holder of 10 patents. His research interests are in new and innovative materials, structures, and process technology of silicon, germanium, and III–V devices and interconnects for VLSI and nanoelectronics. Special areas of his interest are new device structures to continuous-scaling metal–oxide–semiconductor transistors, DRAMs and Flash memory devices to nanometer regime, 3-D ICs with multiple layers of heterogeneous devices, and metal and optical interconnections.

Prof. Saraswat received the Best Paper Award for six of his technical papers. He was a recipient of the Thomas Callinan Award from The Electrochemical Society in 2000 for his contributions to dielectric science and technology, the 2004 IEEE Andrew Grove Award for seminal contributions to silicon process technology, the Inventor Recognition Award from MARCO/FCRP in 2007, and the Technovisionary Award from the India Semiconductor Association in 2007. He is listed by ISI as one of the 250 highly cited authors in his field.