

Antimonide-Based Heterostructure p-Channel MOSFETs With Ni-Alloy Source/Drain

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Abstract—In this letter, we study the formation and electrical properties of Ni-GaSb alloys by direct reaction of Ni with GaSb. It is found that several properties of Ni-antimonide alloys, including low thermal budget processing (300 °C), low Schottky barrier height for holes (~ 0.1 eV), low sheet resistance of Ni-InGaSb ($53 \Omega/\square$), and low specific contact resistivity ($7.6 \times 10^{-7} \Omega\text{cm}^2$), show good progress toward antimonide-based metal source/drain (S/D) p-channel metal-oxide-semiconductor field-effect transistors. Devices with a self-aligned metal S/D were demonstrated, in which heterostructure design is adopted to further improve the performance, e.g., ON/OFF ratio ($>10^4$), subthreshold swing (140 mV/decade), and high effective-field hole mobility of $\sim 510 \text{ cm}^2/\text{Vs}$ at sheet charge density of $2 \times 10^{12} \text{ cm}^{-2}$.

Index Terms—Antimonide semiconductors, metal source/drain (S/D), Ni-GaSb, p-channel MOSFET.

I. INTRODUCTION

ANTIMONIDE-based compound semiconductors have attracted extensive interest for the replacement of silicon in future high-performance, low-power complementary metal-oxide-semiconductor (CMOS) technologies, due to their superior electron and hole transport properties [1], [2]. Although many works have focused on III-V n-channel MOSFETs [3], [4], performance of III-V p-MOSFETs traditionally lagged behind. Recently, high-performance antimonide p-MOSFETs have been demonstrated [5]–[7]. Peak hole mobility $>900 \text{ cm}^2/\text{Vs}$ can be obtained with strained InGaSb p-MOSFETs [6], [7]. This demonstrates the potential of antimonide compound semiconductors for III-V CMOS electronics.

One of the main obstacles for achieving high-performance III-V MOSFETs is the high-resistance source and drain (S/D) contacts. In addition, the poor thermal stability of oxide/GaSb interfaces and poor recovery of crystalline quality after ion implantation makes the S/D formation process with low thermal budget difficult [8]. Metal alloy with III-V compound semiconductors, which enables self-aligned metal S/D formation process, has been demonstrated recently [9], [10].

Manuscript received July 22, 2013; revised August 28, 2013; accepted August 31, 2013. Date of publication September 18, 2013; date of current version October 21, 2013. The review of this letter was arranged by Editor M. Passlack.

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Digital Object Identifier 10.1109/LED.2013.2280615

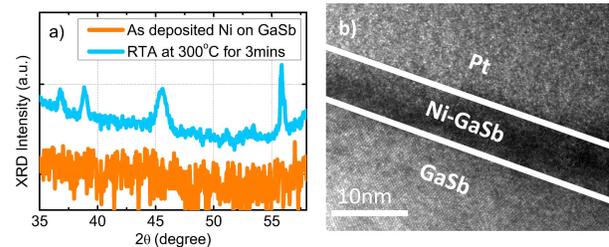


Fig. 1. (a) XRD analysis of 10-nm Ni on GaSb with and without RTA at 300 °C for 3 min. (b) Cross-sectional TEM image of Pt/Ni-GaSb/GaSb.

Initial study on the formation of Ni-GaSb [11] suggests that the selective etching between the metal Ni and Ni-GaSb could potentially enable a self-aligned metal S/D process for antimonide-based p-MOSFETs.

In this letter, we study the formation and properties of Ni-GaSb alloy by direct reaction of Ni with GaSb. A self-aligned, antimonide p-channel MOSFET process with Ni-alloy as S/D is described. The fabricated device shows excellent characteristics.

II. CHARACTERIZATIONS OF Ni-GaSb ALLOYS

After degreasing in solvent and cleaning with diluted HCl (1:1), 10-nm Ni was deposited on bulk GaSb by electron beam evaporation, followed by rapid thermal annealing (RTA) at 300 °C for 3 min. X-ray diffraction (XRD) analysis [Fig. 1(a)] of the annealed sample shows several peaks, which could be attributed to a mixture of binary and ternary phases of Ni-GaSb alloys [11], while those peaks are absent in the control sample. To further confirm the existence of Ni-GaSb alloys and the selective etching of Ni, the sample was subjected to HCl:H₂O (1:5) wet etching to remove unreacted Ni. Pt was then deposited during the sample preparation for transmission electron microscopy (TEM) using a focused ion beam system. Fig. 1(b) shows the cross-sectional TEM image of the Pt/Ni-GaSb/GaSb structure. Ni-GaSb alloy can be clearly identified; the layer thickness is ~ 6 nm. This also demonstrates the selective etching of Ni with respect to Ni-GaSb alloy.

To achieve high I_{ON} and low I_{OFF} at the same time in a metal S/D p-MOSFET, a low Schottky barrier height (SBH) for holes and high SBH for electrons is desired. It is known that the charge neutrality level (E_{CNL}) of GaSb aligns close to the valence band edge of GaSb [8], and exhibits severe Fermi-level pinning. Therefore, Schottky diodes with different contact metals were fabricated to study the SBH of Ni-GaSb

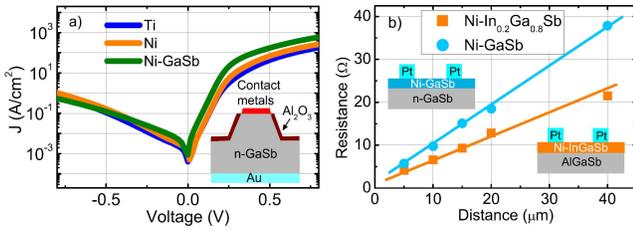


Fig. 2. (a) I - V characteristics of Schottky diodes with different contact metals on n-GaSb. (b) Schematic of structure for TLM and TLM plots of Pt contact to low-sheet-resistance Ni-antimonide alloys.

TABLE I
COMPARISON OF ELECTRICAL PROPERTIES

S/D materials	P+ S/D by ion-implantation	Ni-GaSb	Ni-InGaSb
Thermal budget	350°C 30mins	300°C 3mins	300°C 3mins
Junction depth	>200nm	~6nm	~7nm
R_{sheet} (Ω/\square)	560	87	53
ρ_c (Ωcm^2)	8.7×10^{-6}	3.3×10^{-6}	7.6×10^{-7}

on bulk n-GaSb with carrier concentration of $\sim 5 \times 10^{17} \text{ cm}^{-3}$. Mesa structures were built by wet etching of GaSb with HCl:H₂O:H₂O₂ (50:150:1), and the surfaces were passivated with Al₂O₃ deposited by atomic layer deposition (ALD) to avoid surface conduction. Different contact metals (Ti and Ni) were deposited by electron beam evaporation. To study the Schottky diode between Ni-GaSb/n-GaSb, RTA was performed on the sample with Ni at 300 °C for 3 min to form the Ni-GaSb at the metal/GaSb interface. Finally, Au was deposited on the back of the samples to serve as back contact. Metal/n-GaSb showed very similar Schottky behavior for all the cases in Fig. 2(a), showing high SBH for electrons. For Ni-GaSb, the SBH, extracted from temperature-dependent I - V characteristics, was 0.58 ± 0.06 eV, in agreement with previous report of SBH for different contact metals [11]. The SBH for holes can thus estimated to be ~ 0.1 eV. Such band alignment is important for achieving high I_{ON}/I_{OFF} in p-channel MOSFETs with Ni-GaSb alloy as S/D materials [12].

Achieving a contact with low sheet resistance (R_{sheet}) and low contact resistivity (ρ_c) is essential to further scale antimonide-based p-MOSFETs. N-type bulk GaSb samples were used to confine the conduction in the Ni-GaSb layers. After the blanket formation of Ni-GaSb and selective etching of the unreacted Ni with diluted HCl, a transfer-length method (TLM) test structure was deposited using lift-off of Pt as the contact metals. The same structure was built on a heterostructure sample grown by molecular beam epitaxy [6], which consists of 7-nm undoped In_{0.2}Ga_{0.8}Sb/1 μm Al_{0.8}Ga_{0.2}Sb widebandgap buffer layer on SI GaAs substrate. The same epitaxial wafer was used for transistor fabrication. Fig. 2(b) shows the schematic view of TLM structure, which was isolated by etching, and measurement results. Contact width was 100 μm . The measured ρ_c corresponds to contact resistance of the interface between Pt and Ni-antimonide alloys. Table I

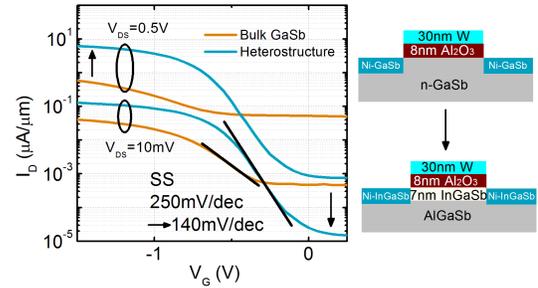


Fig. 3. Transfer characteristics of devices ($L_G \sim 5 \mu\text{m}$) on bulk GaSb substrate and heterostructure stack. Higher ON-current and lower OFF-current were achieved with the heterostructure design.

shows the summary of R_{sheet} and ρ_c , comparing Ni-antimonide alloys and S/D formed by ion implantation of Be [8]. It is shown that with even lower thermal budget (~ 300 °C), Ni-GaSb shows more than seven times reduction in R_{sheet} (87 Ω/\square) and reduced ρ_c ($3.3 \times 10^{-6} \Omega \text{ cm}^2$), as compared with the results from ion implantation. Further reduction in resistance was observed in the heterostructure sample with R_{sheet} of 53 Ω/\square and ρ_c of $7.6 \times 10^{-7} \Omega \text{ cm}^2$, respectively. It has been shown that the resistance of the alloy between Ni and III-Vs, as well as metal contact resistance to the alloy, is correlated with E_{CNL} of the III-V materials and can potentially be engineered [13]. Given that the conducting layer of InGaSb was undoped, the low R_{sheet} and ρ_c could be mainly attributed to E_{CNL} being close to the valence band edge. It proves the potential of such alloys as the S/D materials. R_{sheet} of Ni-antimonide alloy and metal contact property can be further improved with p-type doping.

III. p-MOSFETs WITH Ni-ALLOY S/D

p-MOSFETs with self-aligned Ni-alloy as S/D were fabricated on both a bulk n-GaSb substrate and a heterostructure stack with 7-nm undoped In_{0.2}Ga_{0.8}Sb as the channel. After surface clean, ~ 8 -nm Al₂O₃ was deposited as the gate dielectric by ALD [8]. 30 nm of W was then sputtered, followed by a 350 °C anneal for 1 min in N₂/H₂ (95%/5%) ambient to improve the quality of the gate dielectric and recover the plasma damage. Gate electrodes were patterned using contact lithography, followed by electron beam evaporation of 7-nm Ni. S/D metal pads were deposited by lift-off of 70 nm of Pt. The devices were self-isolated by ring-type structure. RTA was performed at 300 °C for 3 min, followed by etching of unreacted Ni by HCl. Our technology is similar to that described in [10]; the self-aligned S/D was achieved by the selective etching of Ni with respect to Ni-antimonide, as shown in Fig. 1(b).

Drain current density scales with $1/L_G$ with channel length ranging from 100 to 5 μm , showing low external resistance for the set of devices. Fig. 3 shows the transfer characteristics of devices ($L_G \sim 5 \mu\text{m}$). With $V_{DS} = 10$ mV, on the bulk substrate, the I_{ON}/I_{OFF} ratio (~ 50), as well as subthreshold swing (~ 250 mV/decade) of the devices, are largely limited by the I_{ON}/I_{OFF} of the Ni-GaSb/n-GaSb Schottky diode. It is shown that the leakage current is greatly reduced by having a widebandgap buffer layer (Al_{0.8}Ga_{0.2}Sb) beneath the

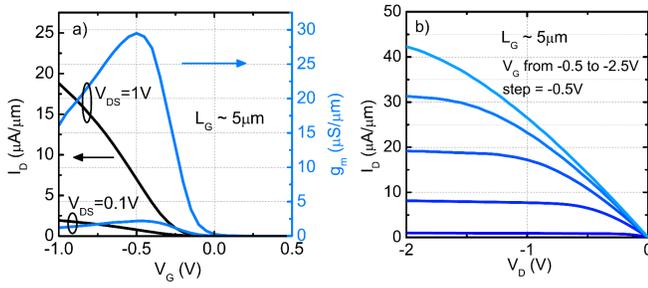


Fig. 4. (a) Transfer and (b) output characteristics of the devices with heterostructure design and Ni-alloy as metal S/D.

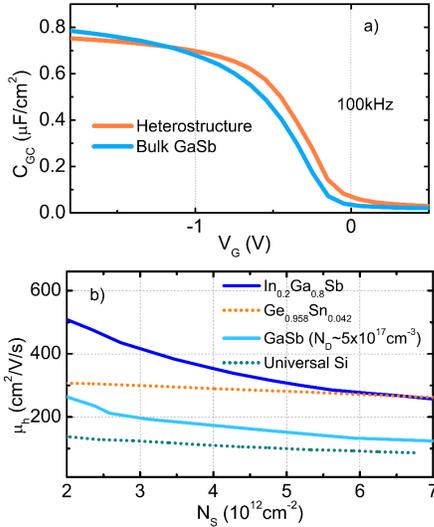


Fig. 5. (a) Gate to channel capacitance (C_{GC}) measured at 100 kHz. (b) Extracted effective-field mobility using split-CV analysis and benchmark it against the mobility in unstrained silicon and strained GeSn.

channel. A high I_{ON}/I_{OFF} of $>10^4$ and subthreshold swing of 140 mV/decade are achieved with the heterostructure design with $V_{DS} = 10$ mV. I_{ON} for the heterostructure design is also higher than that for bulk GaSb due to the reduced extrinsic resistance, the presence of $\sim 0.7\%$ biaxial compressive strain and confinement of carriers in the channel [6]. Fig. 4(a) and (b) shows the transfer and output characteristics of the devices ($L_G \sim 5 \mu\text{m}$) with heterostructure design, which shows a peak transconductance of $29 \mu\text{S}/\mu\text{m}$ at $V_{DS} = 1$ V and I_{ON} of $42 \mu\text{A}/\mu\text{m}$. Further improvement would be possible with the scaling of the gate dielectric thickness. Fig. 5 plots the mobility extracted using split-CV analysis [Fig. 5(a)] and benchmarks it against the mobility in unstrained silicon and strained GeSn p-channel MOSFETs with a metallic S/D [Fig. 5(b)] [14]. In the unstrained case, bulk GaSb gives mobility up to two times higher than that of silicon. The hole mobility is further improved by two times in the heterostructure devices.

IV. CONCLUSION

Studies on the formation and electrical properties of Ni-antimonide formed by direct reaction of Ni with antimonide compounds suggest the potential of Ni-antimonide alloys as an S/D material in antimonide-based p-MOSFETs. A self-aligned process for metal S/D MOSFETs using an epitaxial heterostructure with high hole mobility was developed, and it demonstrates the potential of such S/D design in further channel length scaling of III-V p-channel MOSFETs.

REFERENCES

- [1] G. Dewey, M. K. Hudait, L. Kangho, *et al.*, "Carrier transport in high-mobility III-V quantum-well transistors and performance impact for high-speed low-power logic applications," *IEEE Electron Device Lett.*, vol. 29, no. 10, pp. 1094–1097, Oct. 2008.
- [2] A. Ali, H. Madan, A. Agrawal, *et al.*, "Enhancement-mode antimonide quantum-well MOSFETs with high electron mobility and gigahertz small-signal switching performance," *IEEE Electron Device Lett.*, vol. 32, no. 12, pp. 1689–1691, Dec. 2011.
- [3] D.-H. Kim, T.-W. Kim, R. J. Hill, *et al.*, "High-speed E-mode InAs QW MOSFETs with Al_2O_3 insulator for future RF applications," *IEEE Electron Device Lett.*, vol. 34, no. 2, pp. 196–198, Feb. 2013.
- [4] J. Lin, D. A. Antoniadis, and J. A. del Alamo, "Sub-30 nm InAs quantum-well MOSFETs with self-aligned metal contacts and Sub-1 nm EOT HfO_2 insulator," in *Proc. IEEE IEDM*, Dec. 2012, pp. 757–760.
- [5] M. Xu, R. Wang, and P. D. Ye, "GaSb inversion-mode PMOSFETs with atomic-layer-deposited Al_2O_3 as gate dielectric," *IEEE Electron Device Lett.*, vol. 32, no. 7, pp. 883–885, Jul. 2011.
- [6] A. Nainani, Z. Yuan, T. Krishnamohan, *et al.*, "InGaSb channel p-metal-oxide-semiconductor field effect transistors: Effect of strain and heterostructure design," *J. Appl. Phys.*, vol. 110, pp. 014503-1–014503-9, Jul. 2011.
- [7] K. Takei, M. Madsen, H. Fang, *et al.*, "Nanoscale InGaSb heterostructure membranes on Si substrates for high hole mobility transistors," *Nano Lett.*, vol. 12, no. 4, pp. 2060–2066, Mar. 2012.
- [8] A. Nainani, T. Irisawa, Z. Yuan, *et al.*, "Optimization of the $\text{Al}_2\text{O}_3/\text{GaSb}$ interface and a high-mobility GaSb pMOSFET," *IEEE Trans. Electron Device*, vol. 58, no. 10, pp. 3407–3415, Oct. 2011.
- [9] S. H. Kim, M. Yokoyama, N. Taoka, *et al.*, "Sub-60 nm deeply-scaled channel length extremely-thin body $\text{In}_x\text{Ga}_{1-x}\text{As}$ -on-insulator MOSFETs on Si with Ni-InGaAs metal S/D and MOS interface buffer engineering," in *Proc. Symp. VLSI Technol.*, Jun. 2012, pp. 177–178.
- [10] C. B. Zota, S. H. Kim, Y. Asakura, *et al.*, "Self-aligned metal S/D GaSb p-MOSFETs using Ni-GaSb alloys," in *Proc. 70th Annu. DRC*, Jun. 2012, pp. 71–72.
- [11] C. B. Zota, S.-H. Kim, M. Yokoyama, *et al.*, "Characterization of Ni-GaSb alloys formed by direct reaction of Ni with GaSb," *Appl. Phys. Exp.*, vol. 5, pp. 071201-1–071201-3, Jul. 2012.
- [12] J. M. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1048–1058, May 2006.
- [13] S. H. Kim, M. Yokoyama, N. Taoka, *et al.*, "Self-aligned metal source/drain $\text{In}_x\text{Ga}_{1-x}\text{As}$ n-MOSFETs using Ni-InGaAs alloy," in *Proc. IEEE IEDM*, Dec. 2010, pp. 596–599.
- [14] X. Gong, G. Han, F. Bai, *et al.*, "Germanium-Tin (GeSn) p-channel MOSFETs fabricated on (100) and (111) surface orientations with Sub-400 °C Si_2H_6 passivation," *IEEE Electron Device Lett.*, vol. 34, no. 3, pp. 339–341, Mar. 2013.