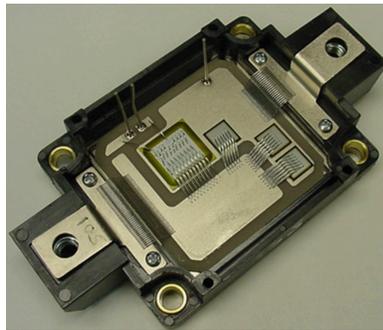




Power Electronics

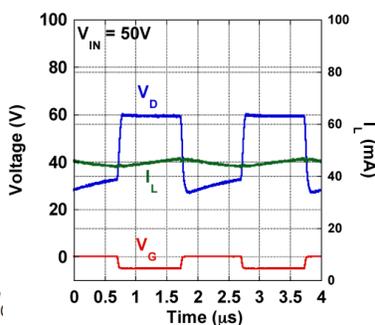
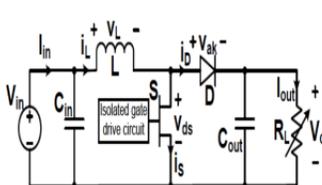
Efficient High-Voltage Silicon/SiC Hybrid Modules

ESTD has developed very efficient medium-voltage power modules by replacing the traditional Si freewheeling diode with SiC Schottky diodes. The SiC junction barrier Schottky (JBS) diodes were rated for 4500 V and replaced the very lossy Si PiN diodes. The combination of SiC diodes and the silicon insulating gate bipolar transistors (IGBT) demonstrated a factor of 7 reduction in turn-on losses and overall better than a factor of 2 in total power dissipation (switching and conduction losses). The SiC JBS diodes have proven extremely reliable and are expected to be commercialized in the near future.



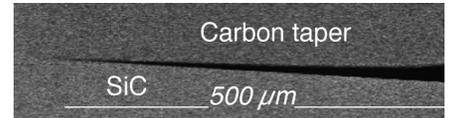
On-Wafer Dynamic Resistance Measurements of GaN Power Switches

GaN high electron mobility transistors (HEMTs) suffer from current collapse, which refers to the increase in on-resistance due to charge trapping in the material when the device is operated under power switching conditions. This is quantified by the dynamic on-resistance of the device, which refers to the ratio of on-resistance values measured under AC and DC operating conditions. ESTD researchers have mated a boost converter power circuit with a probe card to enable the on-wafer device to be inserted into the circuit without packaging. This capability enables the characterization of the switching waveforms and calculation of dynamic on-resistance under realistic AC operating conditions that mimics pulse-width modulation seen in real circuits, enabling optimization of the device structure and an improved approach to reliability testing.

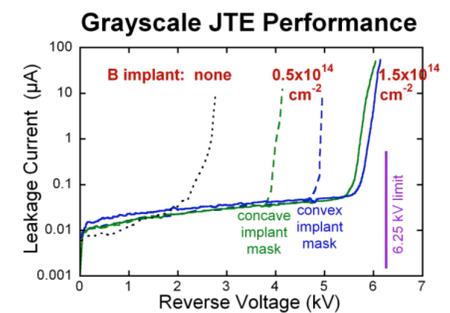


Grayscale Lithography High-Voltage Termination

ESTD researchers invented a simple method that efficiently suppresses electrical breakdown in high-voltage devices. The NRL process employs optics and semiconductor processing to produce a smoothly tapered doping around the terminal. The design of the optical mask directly controls the doping taper width and shape, producing an optimal electrical termination in a single lithographic step.

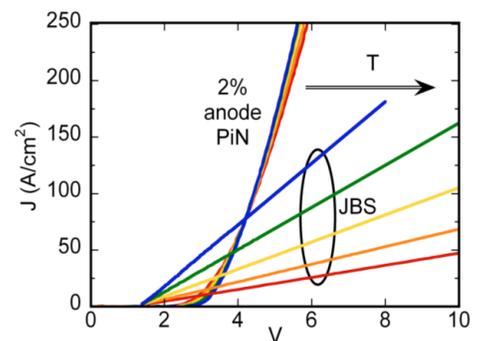


High-voltage diodes made with this NRL process withstood 6.1 kV across only 38 μm of silicon carbide, more than twice the voltage of devices without the NRL process. This grayscale termination process has been applied to other high-voltage device design, such as SiC thyristors.



Nonlinear Current Compression SiC PiN Diodes for Positive Temperature Coefficient

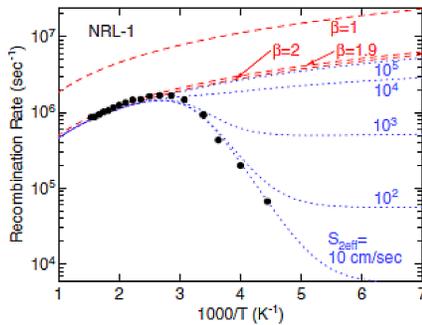
ESTD investigators demonstrated silicon carbide PiN diode rectifiers with positive temperature coefficient in forward-bias operation. Until this work, the one significant limitation of SiC PiN diodes compared with Schottky rectifiers was a negative coefficient of forward voltage drop as the temperature increases. This results in increased current conduction as the temperature rises, which can result in thermal runaway. The power electronics research team has exploited nonlinear current compression within the PiN anodes to achieve a built-in positive temperature coefficient. The resulting SiC PiN diodes can be safely and simply used for extremely high current applications such as massively ganged-parallel rectifier banks where thermal runaway would be catastrophic.



(continued)

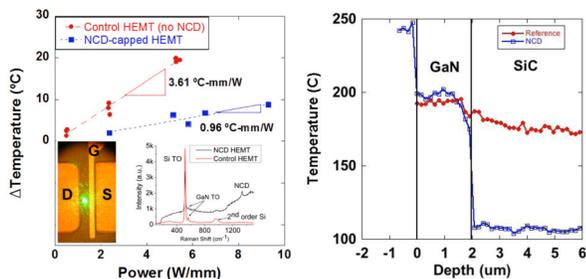
Minority Carrier Lifetime in n-type 4H-SiC Epilayers

While the bulk lifetime killer in 4H-SiC epitaxial drift layers has been identified ($Z_{1/2}$ defect) and its concentration greatly reduced, carrier lifetimes are still too short for device applications. Modeling the carrier lifetime and comparing to temperature-dependent lifetime measurements, it was shown that in low- $Z_{1/2}$ material the lifetime is limited by recombination at the surface and substrate interface. Using the carrier dynamics model employed in analyzing the data, the conditions necessary to achieve long lifetimes were also determined. To achieve lifetimes $>10 \mu\text{s}$ will require very thick epilayers, substantial improvement in surface and interface recombination velocities, and still lower $Z_{1/2}$ concentrations.



3D Temperature Profiling of GaN Power Switches

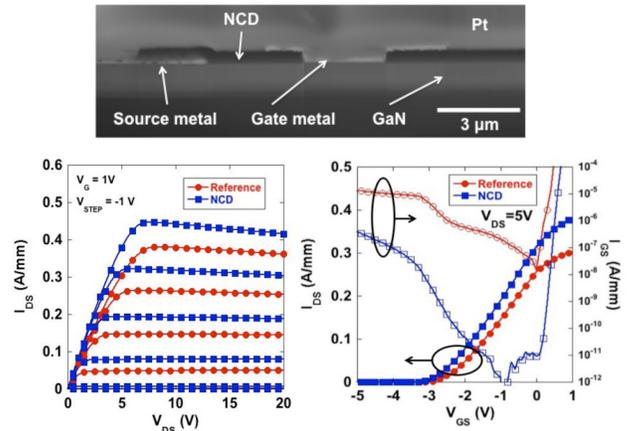
Self-heating of GaN transistors at the high bias conditions experienced in power converter circuits results in decreased efficiency and accelerated device failure. While high thermal conductivity substrates can be used to reduce self-heating, the effectiveness of this approach is limited by the presence of high thermal resistance layers within the device structure. The ESTD



researchers have developed a method to identify and study thermal boundaries in GaN devices using high resolution Raman spectroscopy. This system is capable of $0.2 \mu\text{m}$ resolution in the X, Y, and Z directions, enabling mapping of the temperature distribution in the active device layer structure. The ability to precisely identify the location of high thermal resistance boundaries in the device structure enables NRL scientists to engineer the structure to eliminate these boundaries, thus optimizing the device structure for both performance and heat transfer.

Diamond for Thermal Management in Power Electronics

Diamond has been proposed as an integrated heat sink layer for gallium nitride high electron mobility transistors (HEMTs), but has experienced limited success due to the harsh deposi-



tion conditions and limited sample size. ESTD researchers have developed and patented a new, more reliable and scalable integration scheme referred to as “diamond-before-gate” using NRL’s nanocrystalline diamond (NCD). High-resolution Raman thermography, which was used to generate a 3D map of the temperature in the active layers, indicated a 20% reduction in channel temperature relative to a conventional HEMT. In addition, NRL’s NCD-capped devices have shown a higher current density, lower on-resistance, and improved breakdown voltage, which leads to improved reliability and circuit efficiency.