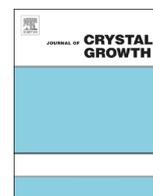




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Strained InGaAs/InAlAs quantum wells for complementary III–V transistors



Brian R. Bennett*, Theresa F. Chick, J. Brad Boos, James G. Champlain, Adrian A. Podpirka

Electronic Science and Technology Division, Naval Research Laboratory, Washington, DC, USA

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ABSTRACT

Quantum wells of InGaAs clad by InAlAs were grown on AlGaAsSb buffer layers by molecular beam epitaxy. The buffer layer lattice parameters were near 6.0 Å, yielding tensile strains up to 2% in the InGaAs and InAlAs. Room-temperature electron mobilities of 9000–11,000 cm²/V s were achieved. Field-effect transistors (FETs) were fabricated and exhibited good DC and RF characteristics. Previous work demonstrated compressively-strained GaSb quantum wells on similar buffer layers with high hole mobilities and good transistor performance. Hence, a single buffer layer of AlGaAsSb should be suitable for complementary circuits comprised of n-channel FETs based on the mature InGaAs/InAlAs technology and p-channel FETs based on high-mobility antimonides.

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1. Introduction

Recently, there has been considerable interest in the potential of III–V field-effect transistors (FETs) for advanced logic applications [1,2]. A III–V high-speed, low-power logic technology could enhance digital circuit functionality and sustain Moore's law for additional generations. When utilized in mixed-signal circuits, a significant reduction in power consumption could also be obtained. For these applications, complementary circuits based on n- and p-channel III–V FETs would be highly desirable due to their low-power, high-speed advantages. A key issue is the composition of the channel and barrier materials for both the n-FET and the p-FET. A strong candidate for the n-FET is a high-mobility InGaAs channel clad by InAlAs barriers. This can take advantage of the mature InP high-electron-mobility transistor (HEMT) technology – so named because InP is usually used as a substrate for lattice-matched or strained InGaAs and InAlAs. Integrated circuits based on InP HEMTs are suitable for a variety of microwave applications including cell phones, cellular base stations, fiber optic systems, radar, radio astronomy, and satellite communications. Quantum wells of InGaAs/InAlAs have a sufficient valence band offset for hole confinement. Hence, one CMOS option is to combine

InGaAs p-FETs and n-FETs. A few groups have investigated p-type modulation doped InGaAs/InAlAs QWs, but the hole mobilities are only 200–400 cm²/V s at room temperature [3–6]. This will limit the performance of InGaAs p-FETs. In contrast, mobilities greater than 2000 cm²/V s have been achieved for strained Ge/SiGe QWs [7]. Therefore, a second option is to combine InGaAs n-FETs with Ge p-FETs to take advantage of the attractive electron and hole mobilities, respectively, in these materials [2]. Integration is a challenge with this approach, however, because of the different crystalline structures and lattice parameters for the two material systems [8,9].

The use of Sb-based materials for both the n- and p-channels is also an attractive possibility since these materials have excellent electronic properties. This combination may enable the use of heterostructures which have the same buffer layer. The use of antimonide/arsenide heterostructures for n-FETs and other electronic devices was reviewed in Ref. [10]. Work on enhancing the hole mobilities for p-FET applications has been encouraging. Confinement and biaxial strain have been used to lift the heavy-hole/light-hole degeneracy, reduce the effective mass, and enhance the hole mobility [3,11]. Room-temperature hole mobilities as high as 1100–1500 cm²/V s have been reported for InSb [12], GaSb [13–15] and InGaSb [16,17]. These antimonide quantum wells have been used in Schottky-barrier p-FETs with good DC and microwave performance [12,18]. In addition, (In)GaSb-channel MOSFETs have been fabricated; they have the attractive advantage of much lower gate leakage current which is a critical requirement in low-power logic

* Corresponding author.

E-mail address: brian.bennett@nrl.navy.mil (B.R. Bennett).

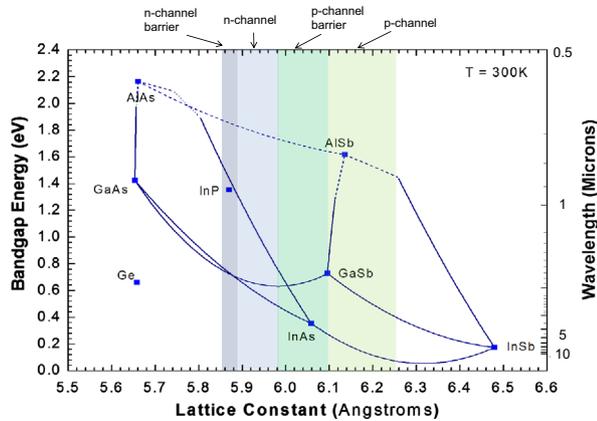


Fig. 1. Energy gap vs. lattice parameter showing regions usually used for channels and barriers in n- and p-channel FETs.

circuits [4,19–21]. The antimonide heterostructures used for p-FETs have type-I band alignments, with substantial conduction as well as valence-band offsets. Hence, a third option for a III–V CMOS is to use antimonide QWs for both n- and p-FETs. For InSb QWs, high-frequency n-FETs have been reported [22]. One potential limitation to InSb QWs for integrated n- and p-FETs is that simulations suggest it may be difficult to attain high I_{ON}/I_{OFF} ratios because of the small band gap and band offsets [23]. We proposed the use of the same InGaSb channel for n- and p-FETs [24,25]. Although high electron mobilities have been achieved [24,26,27], no group has reported a high-performance InGaSb n-FET. A fourth option is to combine p-channel InGaSb with n-channel InAsSb [28–30]. Separate quantum wells are required for the n- and p-channels, but a common buffer layer could be used to avoid mismatches in the coefficients of thermal expansion [31].

In this work, we are exploring a fifth III–V CMOS option: combining the relatively mature InGaAs n-FET technology with high-mobility (In)GaSb for the p-FET. The lattice mismatch between GaSb and InP is almost 4% as shown in Fig. 1. In III–V epitaxy, strains greater than 2% usually lead to highly defective growth which might seem to preclude this material combination. Fortunately, the p-channels are optimized for compressive strains up to 2%. Hence, if n-channel InGaAs/InAlAs quantum wells can tolerate tensile strains of 2%, it could be possible to have a common buffer layer with an intermediate lattice parameter. Fig. 1 shows the most common lattice-constant ranges for the channel and barrier layers in n-channel InGaAs/InAlAs FETs as well as p-channel antimonide FETs. In this work, we investigate AlGaAsSb alloys with lattice parameters near 6.0 Å as buffer layers for InGaAs-channel n-FETs which may subsequently be combined with Sb-based p-FETs using the same buffer layer for CMOS applications.

2. Experimental procedures

The heterostructures studied here are grown by solid-source molecular beam epitaxy (MBE) on semi-insulating (001) InP substrates using a Riber Compact 21T MBE system. A cross-section is shown in Fig. 2. As₂ and Sb₂ are provided by valved cracking cells. The first layer is 160 nm of In_{0.52}Al_{0.48}As lattice matched to InP, followed by a 0.9–2.8 μm digital alloy of Al_{0.8}Ga_{0.2}As_ySb_{1–y}, a 6 nm In_{0.52}Al_{0.48}As barrier, a 15 nm In_xGa_{1–x}As channel ($x=0.64–1.0$), a 5 nm In_{0.52}Al_{0.48}As spacer, Te delta doping [32], a 4 nm In_{0.52}Al_{0.48}As barrier, and a 2 nm In_xGa_{1–x}As cap. (We note that AlGaAsSb will provide a sufficient conduction band offset for electron confinement in the InGaAs. We included the InAlAs barrier layers to make the active region of the device

In _x Ga _{1–x} As 2 nm	
In _{0.52} Al _{0.48} As 4 nm	
In _{0.52} Al _{0.48} As 5 nm	Te δ Doping ↑
In _x Ga _{1–x} As 15 nm	#1,2 $x=0.64$ #3,4 $x=0.8$ #5 $x=1$
In _{0.52} Al _{0.48} As 6 nm (3 nm for #1)	
Al _{0.8} Ga _{0.2} Sb/Al _{0.8} Ga _{0.2} As digital superlattice - not rotated (0.9–28 μm)	
In _{0.52} Al _{0.48} As 0.16 μm	
InP substrate, S.I.(001)	

Fig. 2. Cross-section of InGaAs/InAlAs quantum well in tension on a strain-relaxed AlGaAsSb buffer layer.

similar to conventional InP HEMTs. A recent report showed good electron mobilities in InGaAs quantum wells clad by AlAsSb lattice-matched to InP [33].) The Al_{0.8}Ga_{0.2}As_ySb_{1–y} buffer layers were grown as a short-period superlattice of Al_{0.8}Ga_{0.2}Sb and Al_{0.8}Ga_{0.2}As by toggling the As and Sb shutters while the Al and Ga shutters and the As and Sb valves remained open, allowing better control of composition compared to random alloys [13,34,35]. Short-period superlattices may also aid in the reduction of threading dislocations through the film [36]. The anion ratio was adjusted by changing the length of time the As shutter is open relative to the Sb shutter, e.g. 3.7 s Al_{0.8}Ga_{0.2}Sb/1.3 s Al_{0.8}Ga_{0.2}As. The buffer layer composition dictates the amount of biaxial strain in the thin pseudomorphic InAlAs and InGaAs layers.

The MBE growth temperature is near 450 °C for the InAlAs buffer layer. The temperature is then raised to 510 °C for the Al_{0.8}Ga_{0.2}As_ySb_{1–y} buffer layer, and then reduced to 450 °C for the remaining layers. The InAlAs layers were grown at a rate of 1.0 monolayers (ML)/s, and the InGaAs layers were grown at 0.5 ML/s, as calibrated from reflection high-energy electron diffraction oscillations. Based upon previous results on this MBE system, we expect the layer thicknesses to be uniform to within 1% across the 76-mm-diameter substrate if the wafer is rotated. Table 1 includes relevant parameters for the five MBE growths in this study. The wafers were rotated during the growth of all the layers except the Al_{0.8}Ga_{0.2}Sb/Al_{0.8}Ga_{0.2}As superlattice. This resulted in differing thicknesses of AlGaSb and AlGaAs and different anion mole fractions across each wafer. The buffer layer growth rate was 1.0 ML/s in the center of the wafer, and varied from 0.7 to 1.3 ML/s across the wafer. Several 5 × 5 mm² squares were cleaved from different locations on each wafer to provide a range of samples with varying InGaAs and InAlAs strain in a highly efficient manner.

Hall/van der Pauw transport measurements were performed on a total of 34 samples at 300 K, using magnetic fields of 0.37, 0.55 and 1.0 T. Measurements were performed at two current levels at each B field, and average values are given in this paper with standard deviations usually less than 5%. Room-temperature, 55-point resistivity maps were generated for each wafer from eddy-current measurements using a contactless Leighton 1500 system [37]. Atomic force microscopy (AFM) measurements were performed on two to five samples from each wafer to yield root-mean-square (rms) roughness over 5 × 5 μm² regions for a variety of strains and electron mobilities. X-ray diffraction (XRD) measurements were made on a double-crystal system using Cu-Kα radiation and compared to simulations using dynamical diffraction theory.

Table 1
Growth parameters for the five wafers in this study are given in columns 2–5. Wafers were not rotated during the growth of the buffer layers to yield nonuniformities in quantum well strain, allowing several samples to be cleaved from each wafer. For each wafer, the transport and strain parameters for the sample with the highest room-temperature mobility are given in columns 6–13.

Growth #	x In $\text{In}_x\text{Ga}_{1-x}\text{As}$	Periods in buffer layer	Duty cycle of AlGaSb/AlGaAs (s)	Growth interrupts	Best mobility @300 K ($\text{cm}^2/\text{V s}$)	Density @300 K ($\times 10^{12}$) (cm^{-2})	Mobility @77 K ($\text{cm}^2/\text{V s}$)	Buffer lattice constant (\AA)	Strain in channel (%)	Strain in barrier (%)	rms Roughness (nm)	Sheet resistance (Ω/\square)
1	0.64	777	3.5/1.5	N	3600	1.92	4600	6.000	-1.46	-2.20	0.83	903
2	0.64	1554	3.7/1.3	Y	9900	2.79	14600	5.985	-1.21	-1.96	1.05	226
3	0.80	888	3.7/1.3	Y	10200	1.02	16000	6.000	-0.38	-2.21	0.76	602
4	0.80	888	3.9/1.1	Y	11300	2.08	30000	5.982	-0.08	-1.91	0.87	266
5	1.00	1554	3.7/1.3	Y	9300	3.92	15900	5.968	1.52	-1.68	0.92	171

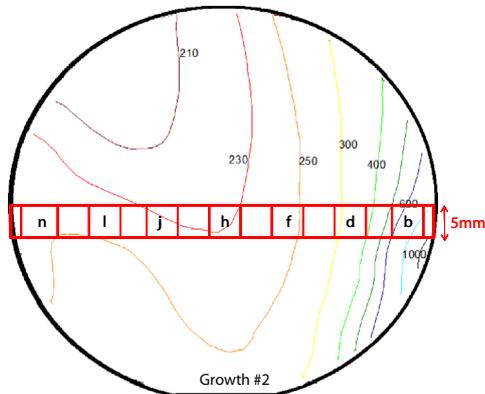


Fig. 3. Resistivity map in units of Ω/\square for growth #2. The gradient across the 76-mm wafer is a result of varying strain in the InGaAs channel and InAlAs barrier layers. The wafer was cleaved into 5×5 mm² squares, as indicated.

3. Results and discussion

In Fig. 3, we show the resistivity map for growth #2, with a 15 nm $\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ channel. The resistivity varied from 197 to $1100 \Omega/\square$. A 5-mm wide strip was cleaved as indicated, yielding thirteen 5×5 mm² samples for characterization. The transport results will be discussed later.

The $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}_y\text{Sb}_{1-y}$ is fully relaxed as confirmed by a reciprocal space map of the asymmetric (224) peaks on sample #3d. In Fig. 4, we show the XRD scan for two pieces (labeled f and j in Fig. 3) from growth #2. The buffer layer consisted of 1554 periods of (3.7 s $\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}/1.3$ s $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$). Peaks are visible for the InP substrate and the short-period superlattice ($n = -1, 0$, and $+1$). Simulations were generated by adjusting the superlattice thicknesses to match the experimental peak positions. The simulation for sample 2f is shown below the experimental data in Fig. 4. The layer thicknesses were 0.43 nm $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$ and 0.86 nm $\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}$, yielding a period of 1.29 nm. Based upon the nominal growth rates, we expect a period of 1.50 nm in the center of wafer #2; f is in a region of lower Al and Ga flux than the center. The buffer layer thickness is 2.00 μm (1554×1.29 nm). The epilayer peaks are all broadened compared to the simulation. For example, the full-width at half-maximum for the $n=0$ superlattice peak is $590''$ for 2f and $500''$ for 2j, compared to $11''$ for the simulation. This broadening is a result of a high density of misfit dislocations required to relax the lattice mismatch with respect to the InP substrate. These dislocations also prevent the observation of peaks from the thin InAlAs and InGaAs layers which are near $+2000$ in the simulated data. Using the superlattice layer thicknesses and Vegard's law (assuming the nominal Al and Ga mole fractions), we calculate the effective quaternary composition to be $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}_{0.33}\text{Sb}_{0.67}$ with a lattice parameter of 5.972 \AA .

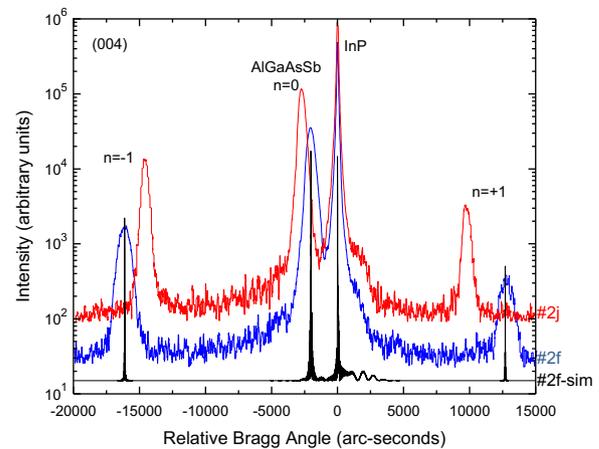


Fig. 4. X-ray diffraction data for samples #2f and #2j and simulation for 2f. The lattice parameter of the buffer layer (and the strain in the channel and barrier layers) is extracted from the peak separations.

The biaxial strain in the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier is -1.76% where we define layers in tension to have negative strain. The $\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ has a larger lattice parameter than the barrier layer. Hence, the tensile strain is smaller, -1.00% . Samples with higher As concentrations in the buffer layer generally exhibited weaker satellite peaks. This indicates that the superlattices are not as well defined but does not necessarily imply lower crystalline quality.

X-ray measurements and simulations were performed on all 34 samples. The AlGaAsSb buffer layers for wafers #3 and #5 were grown with the same superlattice growth times (3.7 s AlGaSb and 1.3 s AlGaAs) and the same As and Sb cell temperatures and valve settings. The growths were performed only one week apart, meaning that the As and Sb fluxes should be similar for the two growths. In Fig. 5, we plot the lattice parameter of the buffer layer vs. the superlattice period for six samples from wafer #3 and seven from wafer #5. They follow the same pattern. As the fluxes of Al and Ga increase, the lattice parameter increases, meaning the fraction of Sb is increasing and the fraction of As is decreasing.¹ One interpretation is that the As is preferentially incorporated and enough Sb is incorporated to maintain the 1:1 V:III stoichiometry [38,39]. The solid curve in Fig. 5 was generated by fixing the AlGaAs thickness at 4.2 \AA and varying the $\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}$ thickness. It matches the trend of the data. The experimental data for wafer #5

¹ The ten concentric cells in the MBE are evenly spaced. Ga is adjacent to Al. Our previous work showed that the Al flux varied by about a factor of two across the 76 mm substrates [13]. We expect a similar variation for Ga, and that the Al and Ga mole fractions are approximately 0.8 and 0.2, respectively. We have less knowledge about the As and Sb nonuniformities. The As and Sb cells are adjacent, so we do not expect the difference in the As and Sb gradients to be a dominant factor in the anion mole fractions of the AlGaAsSb.

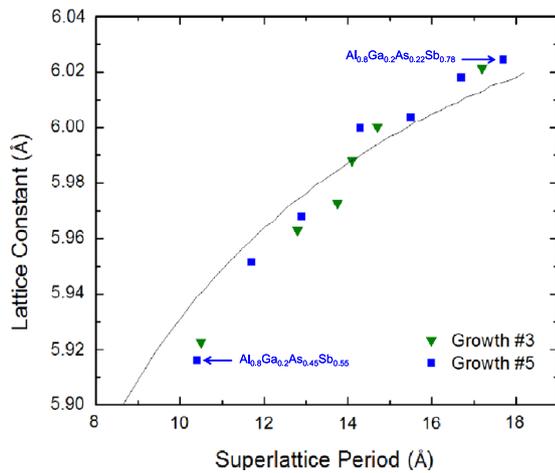


Fig. 5. Buffer layer lattice parameter vs. superlattice period for growths #3 and 5. Solid line is calculated (see text).

ranges from (4.7 Å $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$ /5.7 Å $\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}$, 5.916 Å) to (3.9 Å $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$ /13.8 Å $\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}$, 6.024 Å) with very similar results for wafer #3. Hence, it is primarily the $\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}$ thickness that is varying across each wafer. We also observe a small but consistent decrease in the $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$ thickness as the superlattice period increases which is reflected in the deviations (data points above the curve for SL period of 17–18 Å and data points below the curve for SL period ~ 10 Å) from the calculated curve.

In Fig. 6, we plot the mobility vs. lattice parameter for samples from all five growths. Growths #1 and 2 had 15 nm $\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ channels. Growth #2 had 0.2 s less $\text{Al}_{0.8}\text{Ga}_{0.2}\text{As}$ and 0.2 s more $\text{Al}_{0.8}\text{Ga}_{0.2}\text{Sb}$ per period compared to #1. This should result in an overall shift to larger buffer layer lattice parameters across the wafer. The data in Fig. 6a show that trend, although the range shown for each growth is also a function of which $5 \times 5 \text{ mm}^2$ samples were selected for characterization. For #1, a 3 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ bottom barrier layer was grown, followed by 5 s under an As_2 flux and then the 15 nm channel. For #2, the sequence was 2 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, 30 s As_2 interrupt, 2 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, 30 s As_2 interrupt, 2 nm $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$, 5 s As_2 interrupt, InGaAs channel. The goal of the growth interrupts was to create a smoother starting surface for the channel deposition. The mobility results in Fig. 6a show that the thicker bottom barrier with growth interrupts did indeed result in higher electron mobilities, with values as high as $9900 \text{ cm}^2/\text{V}\cdot\text{s}$ at 300 K. Growths #3–5 used the same bottom barrier layer as #2.

In Fig. 6b, we plot the mobility for growths #3 and #4 which had 15 nm $\text{In}_{0.80}\text{Ga}_{0.20}\text{As}$ channels. The growths were nominally identical except that the GaTe shutter was open for 120 s for #4 compared to 60 s for #3. (The $\text{AlGaSb}/\text{AlGaAs}$ duty cycles were also different but that only affects the range of samples.) As expected, the measured densities for #4 were higher: $\sim 2 \times 10^{12}/\text{cm}^2$ compared to $\sim 1 \times 10^{12}/\text{cm}^2$ for #3. The room-temperature mobilities peak at lattice parameters of 5.97–6.00 Å, similar to the results of growth #2. The highest values were $10,200 \text{ cm}^2/\text{V}\cdot\text{s}$ for #3 and $11,300 \text{ cm}^2/\text{V}\cdot\text{s}$ for #4. A pure InAs channel was used for growth #5; the mobilities are plotted in Fig. 6c. The pattern is similar to the other growths, with a peak mobility of $9300 \text{ cm}^2/\text{V}\cdot\text{s}$ at a lattice parameter of 5.97 Å.

For all three channel compositions (growths #2–5), room-temperature mobilities of $9000\text{--}11,000 \text{ cm}^2/\text{V}\cdot\text{s}$ were achieved; these values are comparable to the state-of-the-art for InP HEMT structures. Our samples include heterostructures with the InGaAs channel in tension, compression, and nearly lattice-matched to the buffer layer. The mobilities are consistent with the fact that strain effects on the band structure of n-channel quantum wells are

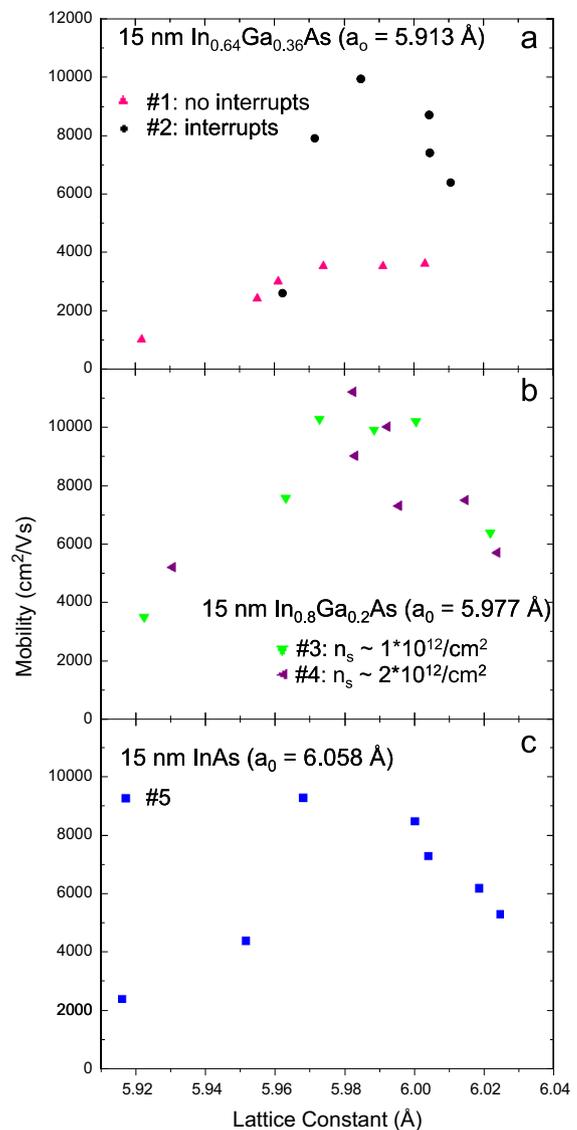


Fig. 6. Room-temperature mobility as a function of buffer layer lattice parameter for samples from all five growths. Peak mobilities are achieved for lattice parameters of 5.97–6.00 Å. Mobility decreases for smaller lattice parameters due to roughness in the buffer layers. For larger lattice parameters, mobility decreases due to high tensile strains ($> 2\%$) in the InAlAs barriers.

expected to be less pronounced than for p-channel quantum wells where compressive strain can give a large mobility enhancement [16]. We achieved high mobilities for both the 888- and 1554-period superlattices, suggesting that the buffer layer thickness is not a critical parameter over the range investigated. The highest values of mobility are found for buffer layer lattice parameters of 5.97–6.00 Å. For smaller or larger lattice parameters, the mobility drops substantially. The decrease for larger lattice parameters was expected because of the large strains in the InAlAs and InGaAs layers. The $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier layers have a lattice parameter of 5.869 Å and are in tension. For a 6.01 Å buffer layer, the strain is -2.41% . For buffer layers with smaller lattice parameters, the strain is lower. For the 6.01 Å buffer layer, the channel strains vary from -1.65% for the $\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ channel to -0.55% for the $\text{In}_{0.80}\text{Ga}_{0.20}\text{As}$ channel and $+0.81\%$ for the InAs channel. Given the larger strains for the InAlAs barriers compared to the InGaAs channel and the similar results at the different channel compositions, it seems likely that the InAlAs layers exceed the critical layer thickness for the larger buffer layer lattice parameters, resulting in the formation of additional misfit dislocations and a degradation

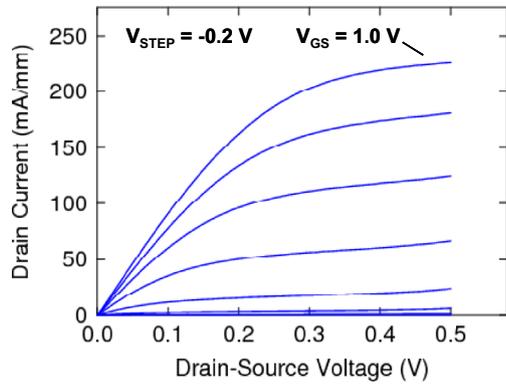


Fig. 7. FET drain characteristics for $\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ -channel HEMT in tension (growth #2) with $L_G=100$ nm and $W_G=31$ μm .

in mobility. As can be seen in Table 1, high mobilities can be achieved for InAlAs strains up to -2.2% . Most previous work on strained InGaAs/InAlAs QWs for HEMTs focused on compressive strain in the InGaAs channel. A few studies included strained InAlAs barriers [40,41].

For lattice parameters of $5.92\text{--}5.96$ Å, strains in the InGaAs and InAlAs layers are smaller. For example, for a 5.94 Å buffer layer an $\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ channel has a strain of -0.46% and an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier has a strain of -1.21% . Hence, it is unlikely that strain-induced misfit dislocations are causing the lower mobilities in this range. AFM measurements show rougher surfaces for all samples with buffer layers which have lattice parameters less than 5.96 Å, with 5×5 μm^2 rms roughness values between 1.3 and 3.1 nm. In contrast, samples with buffer layer lattice parameters greater than 5.96 Å have rms values between 0.8 and 1.1 nm. The AFM images reveal surface undulations with amplitudes less than 2 nm. These may arise from the Asaro–Tiller–Grinfeld instability as observed by Gendry et al. and Ponchet et al. [42,43]. These earlier studies examined tensile-strained InGaAs on InP. In our case, the instability probably results from the tensile-strained InAlAs layers grown on fully relaxed AlGaAsSb buffer layers. These rms roughness values of ~ 1 nm are as good or better than what was measured for InAs-channel HEMT structures on Al(Ga)Sb buffer layers and GaAs or InP substrates and are fully compatible with monolithic-microwave integrated circuit (MMIC) processing [44,45]. These results do not imply that smooth buffer layers cannot be grown in the $5.92\text{--}5.96$ Å regime. The optimal growth temperatures for arsenides are generally higher than for antimonides. Higher buffer layer growth temperatures might yield smoother layers in this range with smaller lattice parameters and higher arsenide mole fractions. Our goal in this work, however, is to have buffer layers with lattice parameters near 6.0 Å. Hence, we did not attempt to optimize the growth conditions for the smaller lattice parameters.

Material from growth #2 ($\text{In}_{0.64}\text{Ga}_{0.36}\text{As}$ channel) was processed into HEMTs. The room-temperature sheet density and mobility were $3.5 \times 10^{12}/\text{cm}^2$ and 7900 $\text{cm}^2/\text{V}\cdot\text{s}$, respectively. The HEMTs were fabricated using a Pd/Pt/Au alloyed source-drain metallization and a Ti/Au gate metallization using standard lithography and liftoff techniques. A typical set of drain characteristics for a HEMT with a 100 nm gate length is shown in Fig. 7. For this device, the gate width is 31 μm and the source-drain spacing is 1.4 μm . The low-field source-drain resistance at $V_{GS}=1.0$ V is 1.1 $\Omega\cdot\text{mm}$ and the threshold voltage is 0.1 V. A maximum DC transconductance of 300 mS/mm is measured at $V_{DS}=0.3$ V. Using S-parameter measurements at $V_{DS}=0.8$ V and $V_{GS}=0.4$ V, an f_T of 160 GHz and an f_{max} of 150 GHz are obtained on a HEMT with a 90 nm gate length after removal of the gate bond capacitance. This corresponds to an $f_T\text{--}L_g$ product of 14 GHz- μm . At this bias

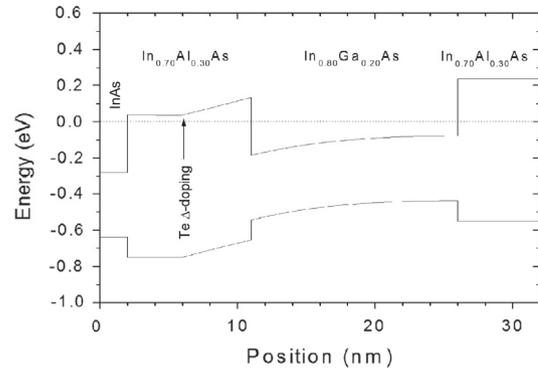


Fig. 8. Calculated band structure of $\text{In}_{0.8}\text{Ga}_{0.2}\text{As}/\text{In}_{0.7}\text{Al}_{0.3}\text{As}$ QW. The conduction band offset is 316 meV; the electron sheet density is $1.4 \times 10^{12}/\text{cm}^2$.

condition, the gate leakage current was 1.4 $\mu\text{A}/\text{mm}$. The performance of these devices is currently limited by a relatively high contact resistance; reduction of the contact resistance should lead to higher f_T values. The key breakthrough here is that the layers are in tension and hence compatible with p-channel FETs on a common buffer layer.

Our recent work demonstrated high-mobility ($1000\text{--}1500$ $\text{cm}^2/\text{V}\cdot\text{s}$) GaSb QWs for compressive strains as high as 2.3% [14]. Hence, the $5.97\text{--}6.00$ Å AlGaAsSb buffer layers demonstrated here could be used with GaSb-channel p-FETs. It may be desirable to use InGaSb alloys for the p-channel [23]. In that case, buffer layers with larger lattice parameters ($6.0\text{--}6.1$ Å) will be needed to avoid excessive lattice mismatch with the InGaSb. At these larger lattice parameters, however, the lattice mismatch in the $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barriers will be too large. An alternative is to use barriers with higher InAs mole fractions. The trade-off is that the conduction band offset will be smaller. To explore this option, we simulated a quantum well with $\text{In}_{0.7}\text{Al}_{0.3}\text{As}$ barriers and an $\text{In}_{0.80}\text{Ga}_{0.20}\text{As}$ well on a 6.05 Å AlGaAsSb buffer layer. The tensile strains in the barrier and channel are -1.87% and -1.21% , respectively. The band structure was calculated using the NextNano program [46] and is shown in Fig. 8. The conduction band offset is 316 meV. This value is smaller than the offset for an $\text{In}_{0.52}\text{Al}_{0.48}\text{As}/\text{In}_{0.80}\text{Ga}_{0.20}\text{As}$ QW (570 meV), but may be sufficient for FET applications. It is larger than the 200 meV offset for $\text{In}_{0.15}\text{Al}_{0.85}\text{Sb}/\text{InSb}$ QWs used in high-performance FETs [47]. Higher conduction band offsets could be achieved with InGaAs/AlGaAsSb quantum wells, but this would not take full advantage of the maturity of the InGaAs/InAlAs HEMT technology.

4. Summary

We have demonstrated that InGaAs/InAlAs QWs with InAlAs barriers in $\sim 2\%$ tension and InGaAs wells in $\sim 1.5\%$ tension to $\sim 1.5\%$ compression can be successfully grown on AlGaAsSb buffer layers with smooth surfaces, high mobilities, and good FET performance. Using epitaxial regrowth [48], it should be possible to integrate InGaAs n-FETs with compressively-strained (In)GaSb p-FETs on a common AlGaAsSb buffer layer. This combination would have much higher hole mobility compared to the n-InGaAs/p-InGaAs CMOS option, and higher I_{ON}/I_{OFF} ratios than are likely with an n-InSb/p-InSb system. It could potentially be grown on a Si substrate and incorporate oxides from atomic layer deposition to form n-InGaAs MOSFETs [49] and p-(In)GaSb MOSFETs [20,50,51]. The implementation of epitaxial regrowth on a common lattice-constant buffer layer may ease the integration complexity of

n- and p-channel FETs and represents a viable path towards high performance III–V CMOS logic.

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